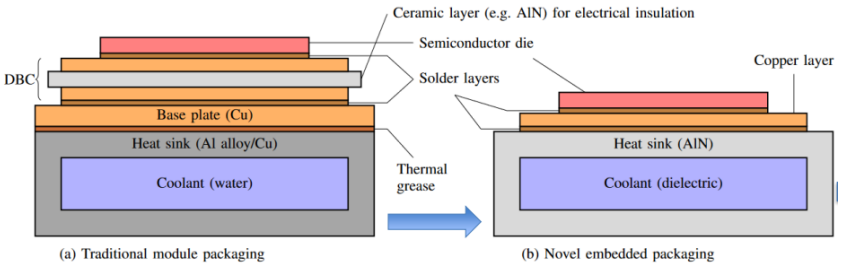
Novel Packaging with Direct Dielectric Liquid Cooling for High Voltage Application

CONTEXT

Standard practice in power electronics packaging is to attach semiconductor die to a carrier ceramic structure which is further attached to baseplate, which is mounted to the heatsink. The ceramic structure is sized according to the required electric insulation voltage between the device and baseplate/heatsink. This ceramic substrate is in the main thermal extraction path of the energy dissipated within semiconductor die. The requirements for insulation between the die and base plate increase for medium and high voltage applications, whether for single device or series device connection within one package. Therefore the thickness of the ceramic substrate has to increase thus degrading thermal performance of the package. In case of series connected devices common base plate also add to common mode coupling between the devices in the package.



TECHNOLOGY DESCRIPTION

It is proposed to incorporate cooling channels within the thickness of the ceramic substrate and use cooling liquid with a similar electric conductivity to the ceramic substrate to decouple the relation between thickness required for insulation and resulting thermal resistance. To create the cooling channel the overall ceramic substrate thickness has to be increased but the thickness under the semiconductor would mainly be governed by mechanical rather than electrical constrains. Therefore, total thermal extraction path would be decoupled from insulation requirements. This approach also eliminates common base plate thus reducing common mode coupling between the devices in the same package.

Prototypes for experimental validation of the concept has been fabricated.

APPLICATION DOMAIN

Packaging for high voltage application

Packaging for devices with breakdown voltage above 10kV

Packaging for series connected devices which require high isolation to ground

ADVANTAGES

Better thermal management of semiconductor die temperature

Decoupled Electrical and Thermal Constraint

Increased power density of semiconductor package

Reduced Common Mode Coupling

TRL SCALE

DELIVERABLES

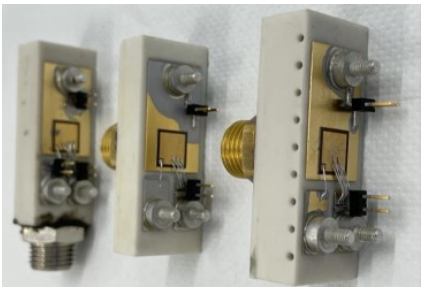
PATENT PCT/FR2018/050197

Technical Reports

Experimental Prototypes

SCIENTIFIC REFERENCE

None



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