



PROMOTiON
PROGRESS ON MESHED HVDC
OFFSHORE TRANSMISSION
NETWORKS



WP9 T9.7/T9.8

Demonstration of Non-selective strategies for Meshed HVDC networks

03-04/09/2020



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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

North Sea Grid for the European New Deal

How to unlock Europe's Offshore Wind potential – a deployment plan for meshed HVDC grid



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Research group leader

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• EXPERIENCE

- PhD in electrical engineering with Valeo, research on starter-alternator control
- 10-years with Alstom Transport as motor control expert
- 6-years with SuperGrid Institute as power converter control engineer and then modelling and simulation group leader

• PROJECT ROLE

- Coordination of the real-time simulation platform of SuperGrid Institute
- Technical review of specifications and test results

CONTENT

5' - CONTEXT

- Objectives
- Roadmap

25' - NON-SELECTIVE PROTECTION STRATEGIES

- Generalities
- Non-selective fault clearing strategies
 - Focus on CBS: Converter breaker strategy
 - Focus on FBS: Full-bridge converter-based strategy

HARDWARE-IN-THE-LOOP DEMONSTRATION

- 40' - Scope
- 30' - Results

5' - CONCLUSION

15' - Q&A session



CONTEXT



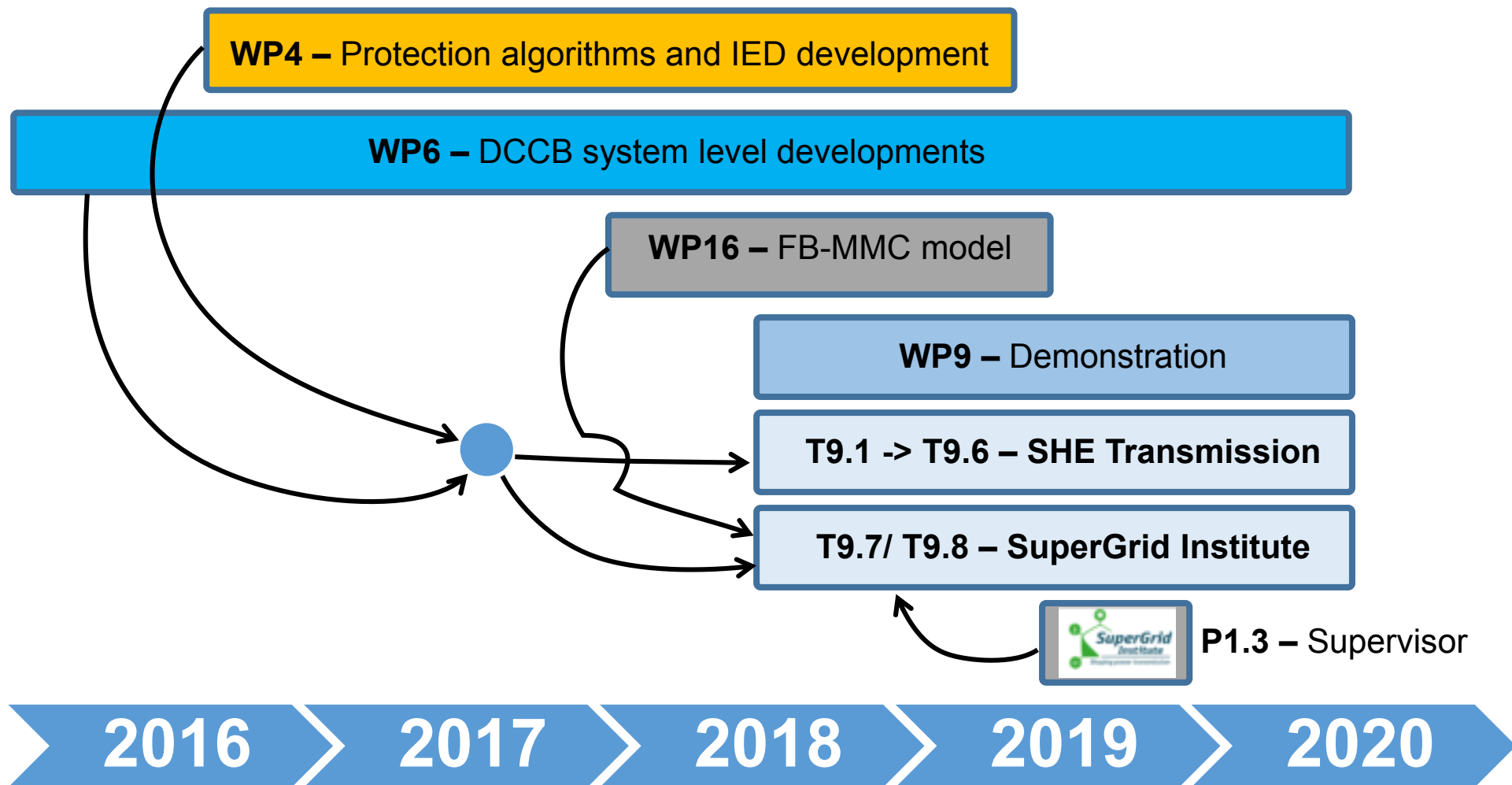
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WP9 Objectives

- Integrate IED prototypes (from WP4) and DCCB models (from WP6) in RTS environments
- Develop DC grid benchmark models and test procedures for protection system testing
- Demonstrate protection system performance using HIL testing
 - Primary sequence
 - Backup sequences
 - System level consequences of protection failure
- Demonstrate equipment interoperability
 - Different DCCB technologies (HSS, DCCB)
 - Different MMC technologies (HB-MMC or FB-MMC)
 - Prototyped IEDs
 - Standard communication protocol (IEC61850)
- Demonstrate DC grid restoration performance (after fault clearing process)
 - DC grid control (station and central supervisors)
 - IEDs (Hardware-In-the-Loop) or in the simulation (Software-In-the-Loop)

CONTEXT

WP9 Framework





NON-SELECTIVE PROTECTION STRATEGIES



Alberto Bertinato



Pascal Torwelle



Philipp Ruffing



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How to unlock Europe's Offshore Wind potential – a deployment plan for meshed HVDC grid



Alberto Bertinato

Research Group Leader - Supergrid Architecture Principles

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• EXPERIENCE

- DC grid protection
- DC grid operation
- AC high voltage substation equipment

• PROJECT ROLE

- Lead of Deliverable 4.3
- Support to WP4, WP9, WP12
- Support for Short Term Project Clean Stream Energy Hub Bornholm



Alberto Bertinato

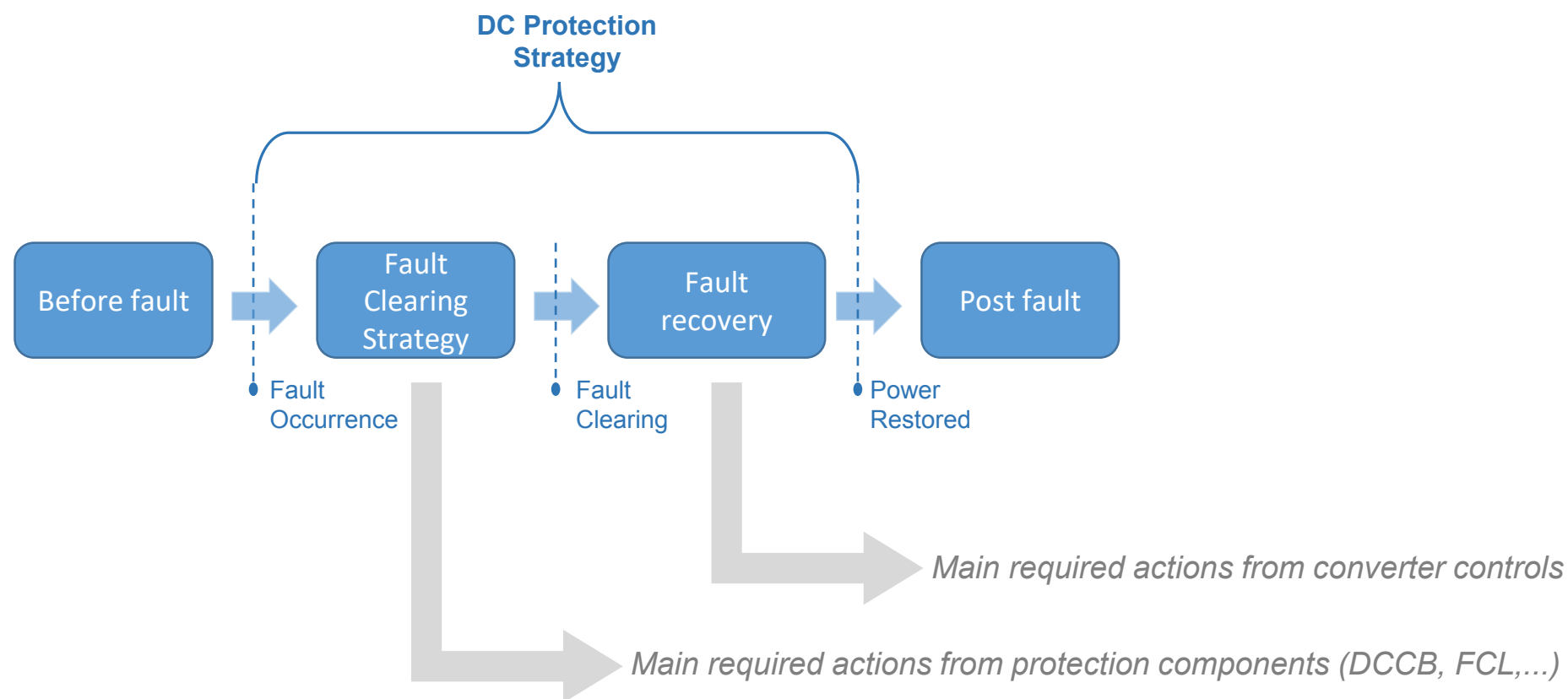
INTRODUCTION TO DC PROTECTION STRATEGIES



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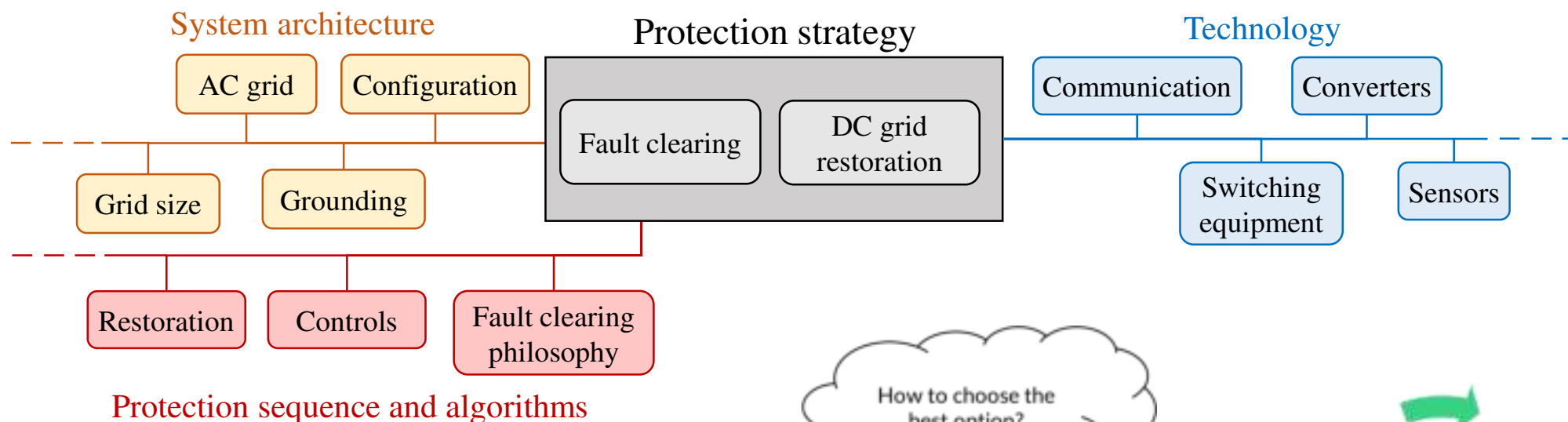
DC Protection Strategy Generalities

- What is meant by DC protection strategy ?



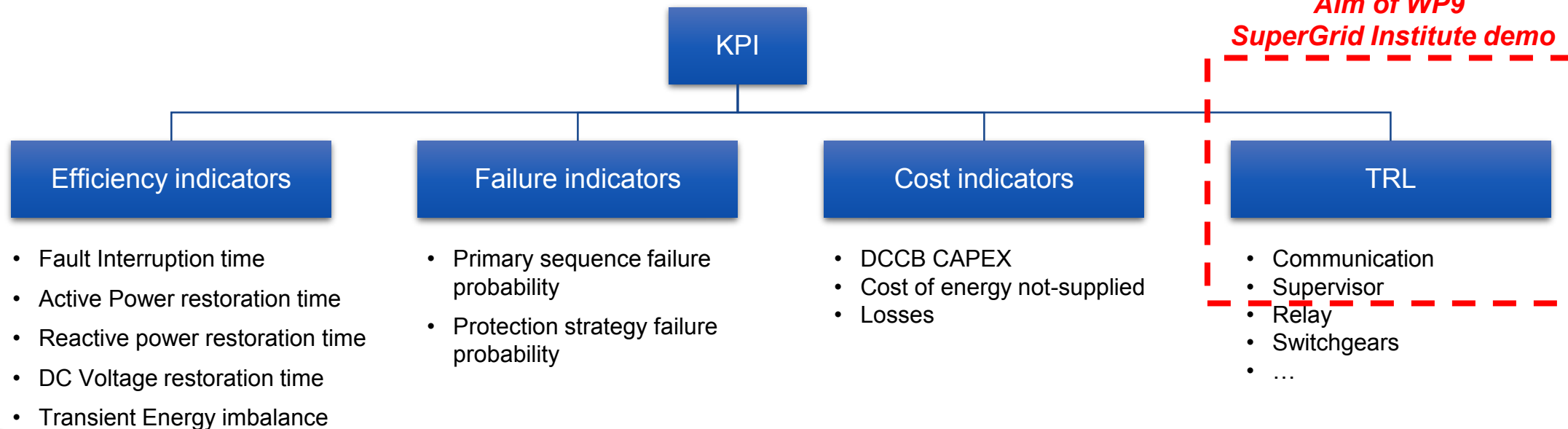
DC Protection Strategy Generalities

- The DC protection strategy is the combination of three key elements:



DC Protection Strategy Generalities

- Proposal of KPIs families
 - ✓ Measure the impact a protection strategy can cause to the DC system
 - ✓ Measure the reliability of the protection strategy
 - ✓ Find the optimum from a techno-economic point of view
 - ✓ Technological Readiness Level of protection equipment



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• EXPERIENCE

- M.Sc. Electrical Power Engineering, LUH Hannover
- Currently: Last year of PhD at Supergrid Institute in cooperation with University Grenoble Alpes, research interest: HVDC grid protection

• PROJECT ROLE

- Support to WP4, Task T4.3



Pascal Torwelle

Converter Breaker Strategy



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OUTLINE

- Introduction
- Protection components and layout
- Primary sequence
- Backup sequence
- Switchgear requirements
- Conclusions



CONVERTER BREAKER STRATEGY

Introduction

Fault Clearing Strategies

Selective fault clearing

Partially selective fault clearing

Non-selective fault clearing



- Converter Breaker Strategy
- Proposed by SuperGrid Institute in PROMOTioN project WP4

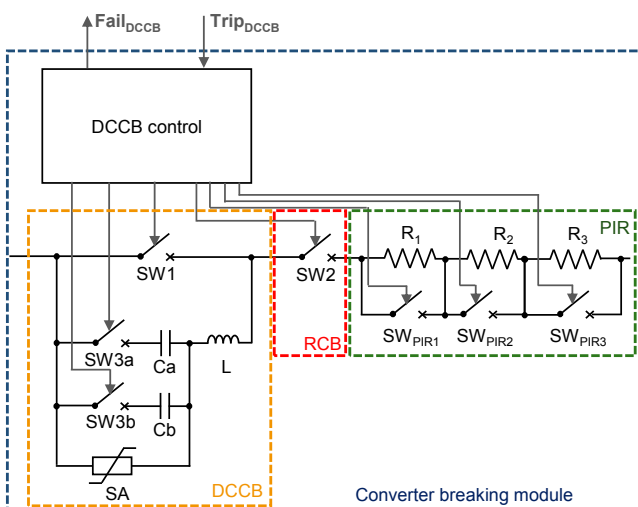


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OFFSHORE TRANSMISSION
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Protection components and layout

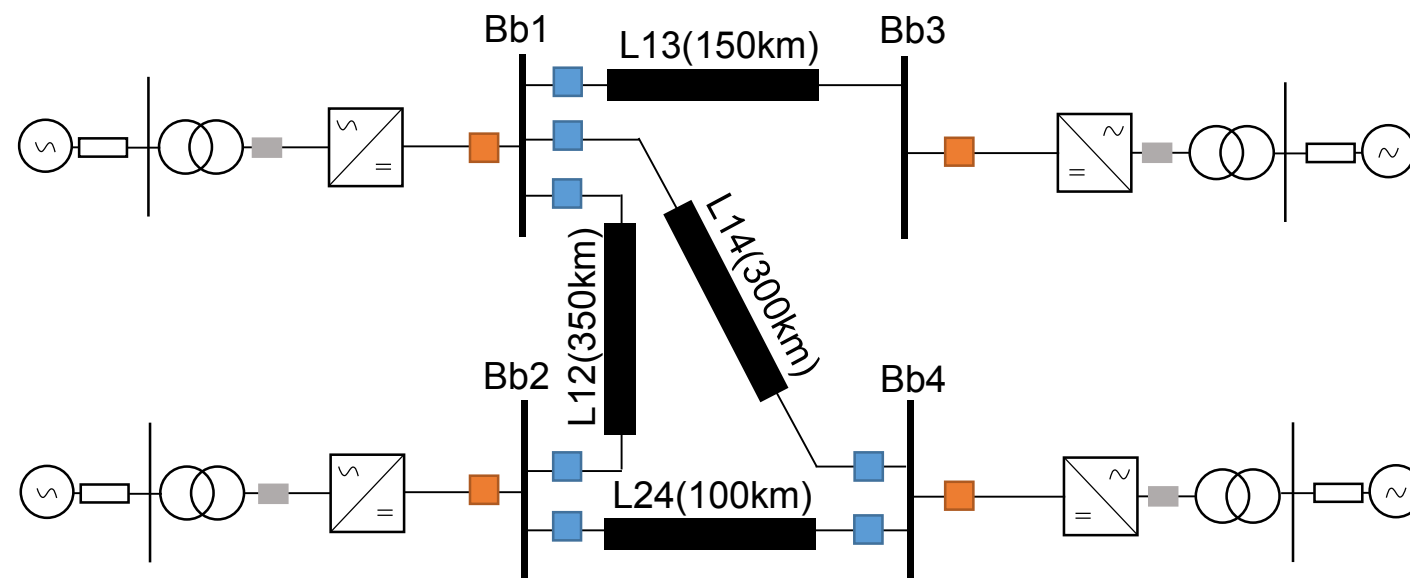
Line breaker module **LB**
installed at each line end

Converter breaker module **CB**
installed at each
converter output



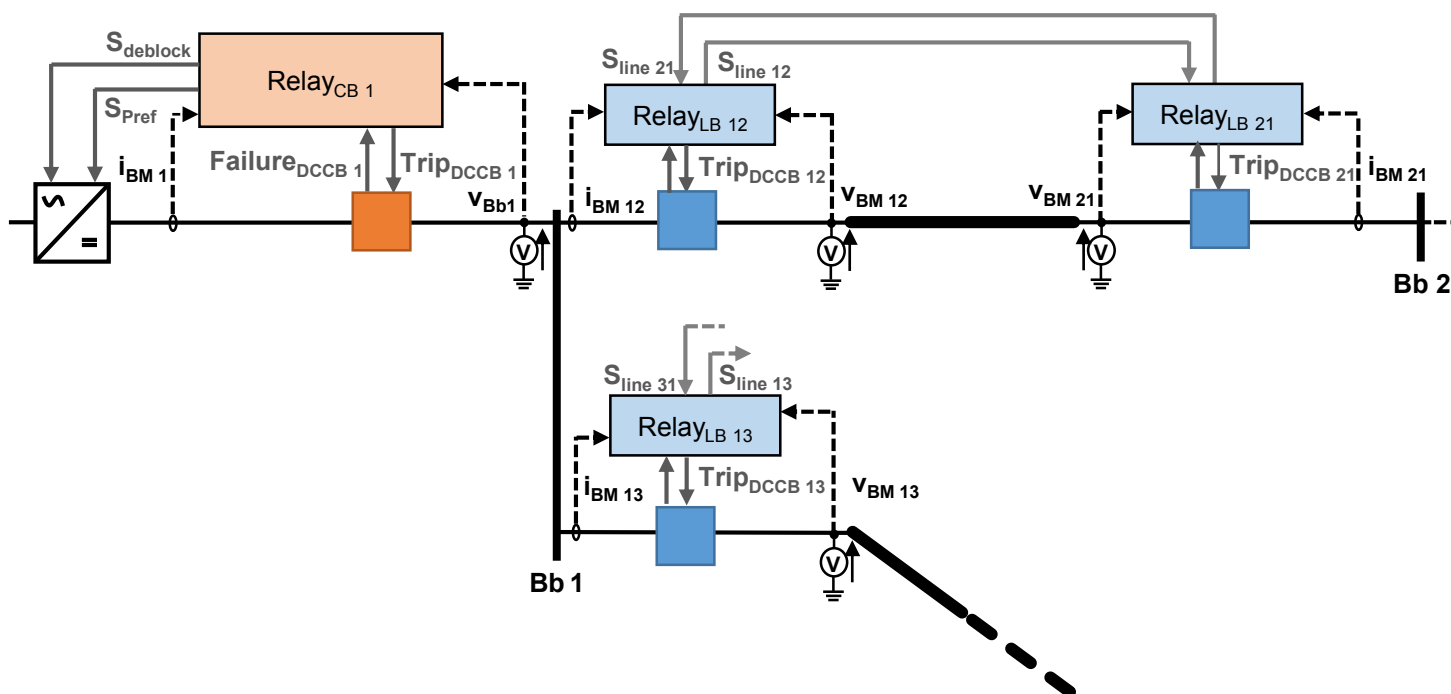
DCCB: DC circuit breaker

RCB: Residual current breaker



Protection components and layout

Sensor measurement and relay communications



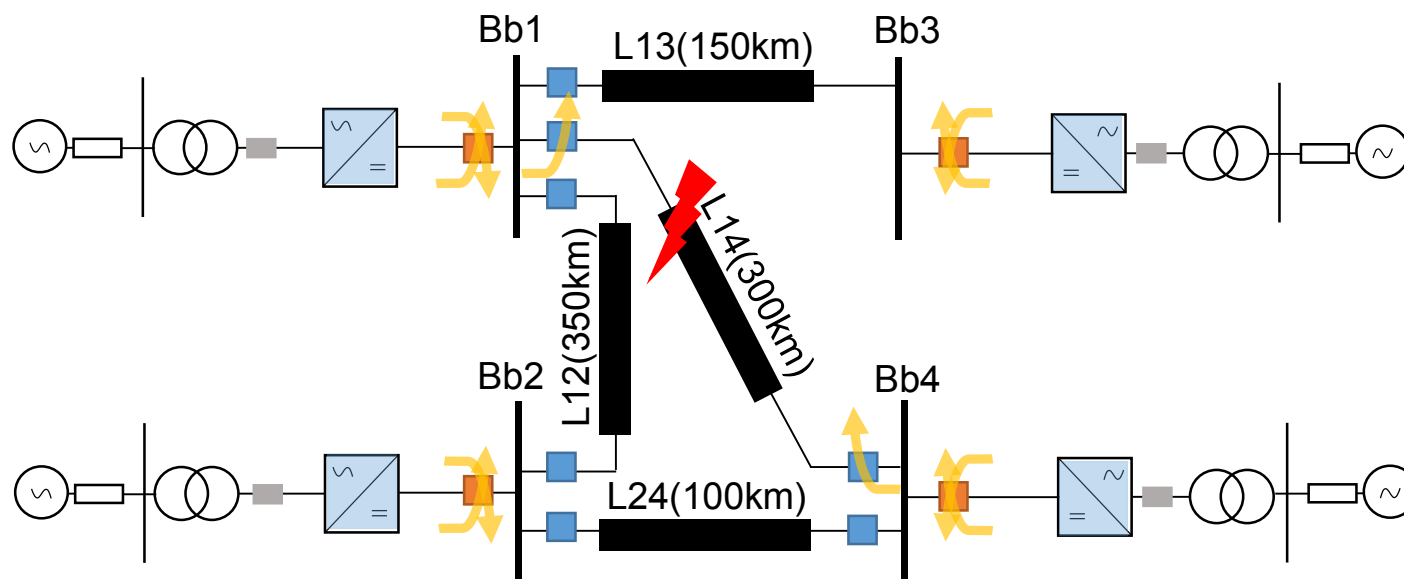
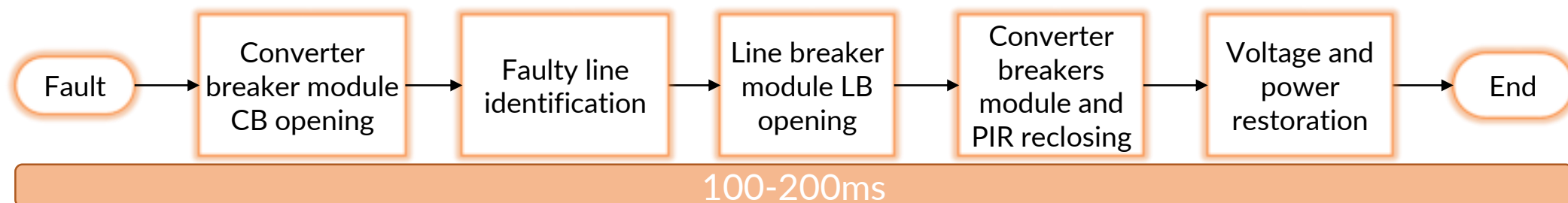
- **CB relay**

- Voltage and current measurements
- Communication with breaking module
- Communication with MMC

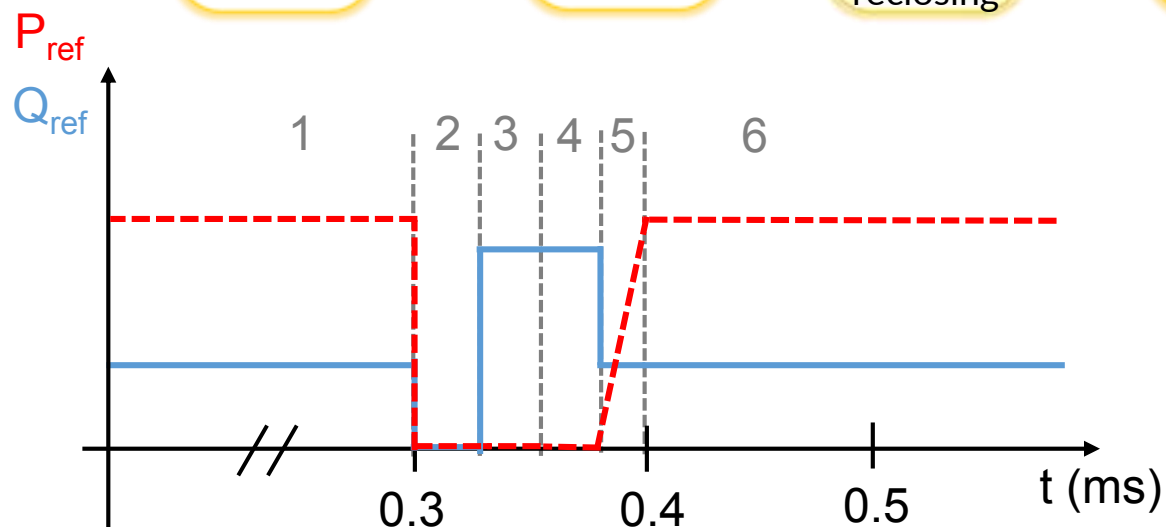
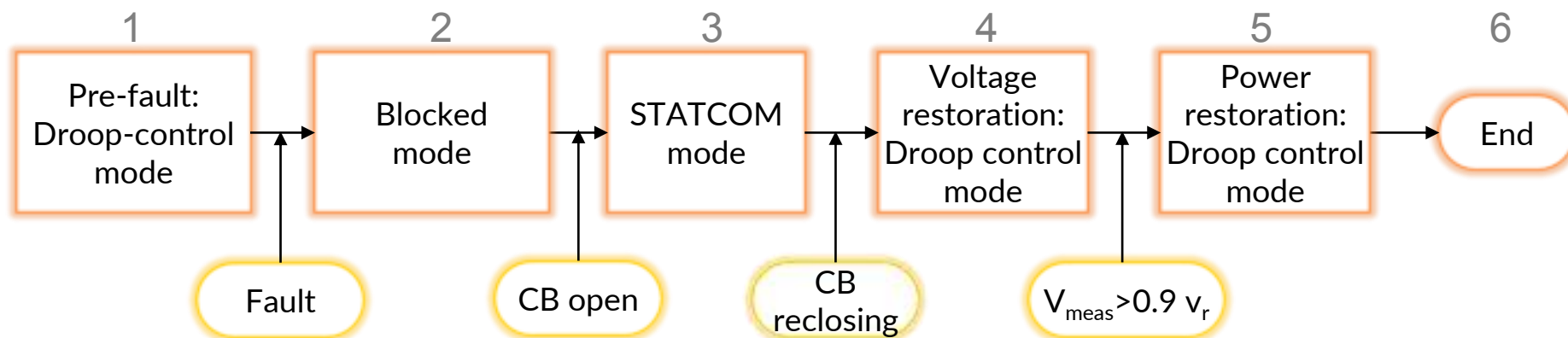
- **LB relay**

- Voltage and current measurements
- Communication with breaking module
- Communication with remote line end

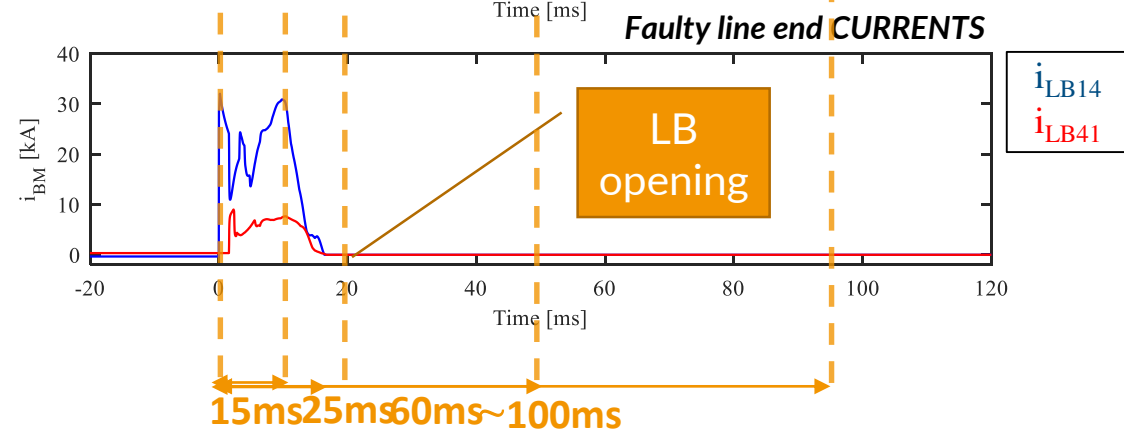
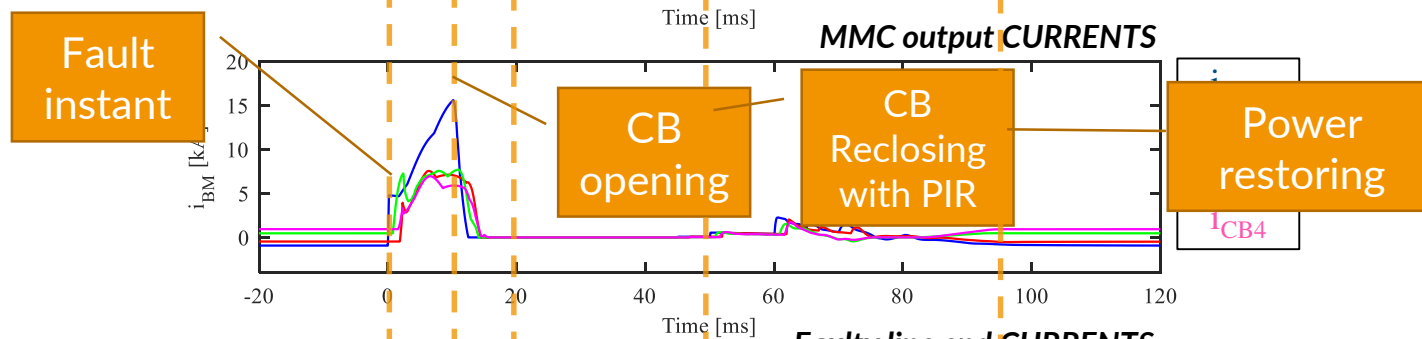
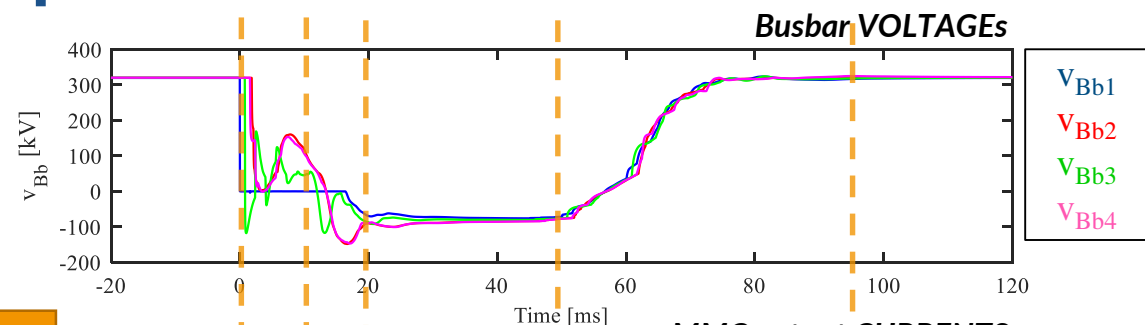
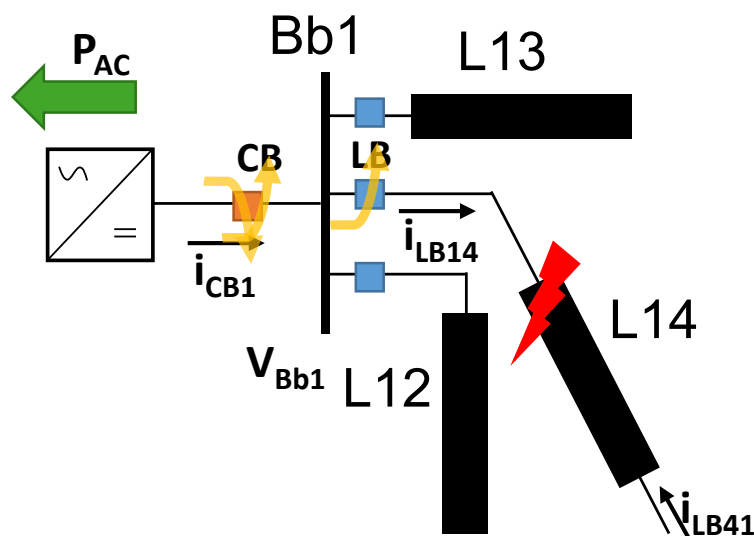
Primary sequence



MMC fault ride through operation modes

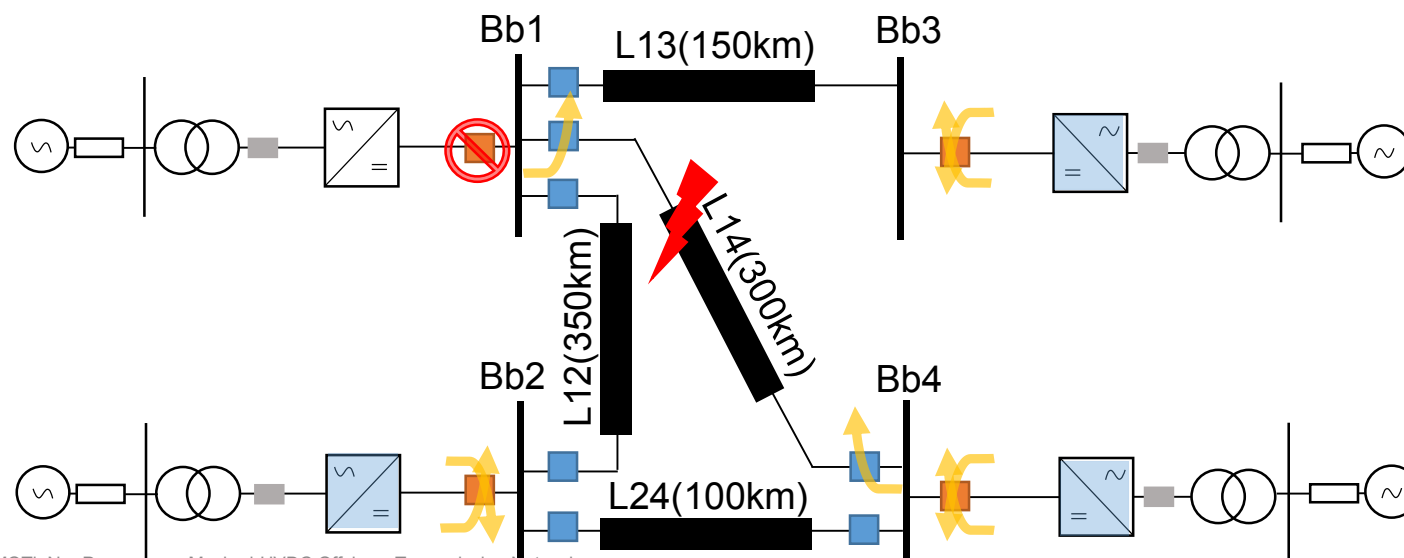
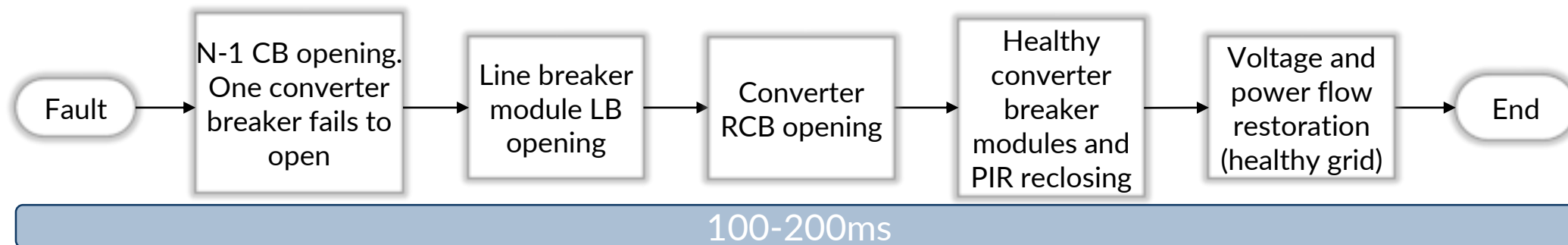


Simulation of the primary sequence



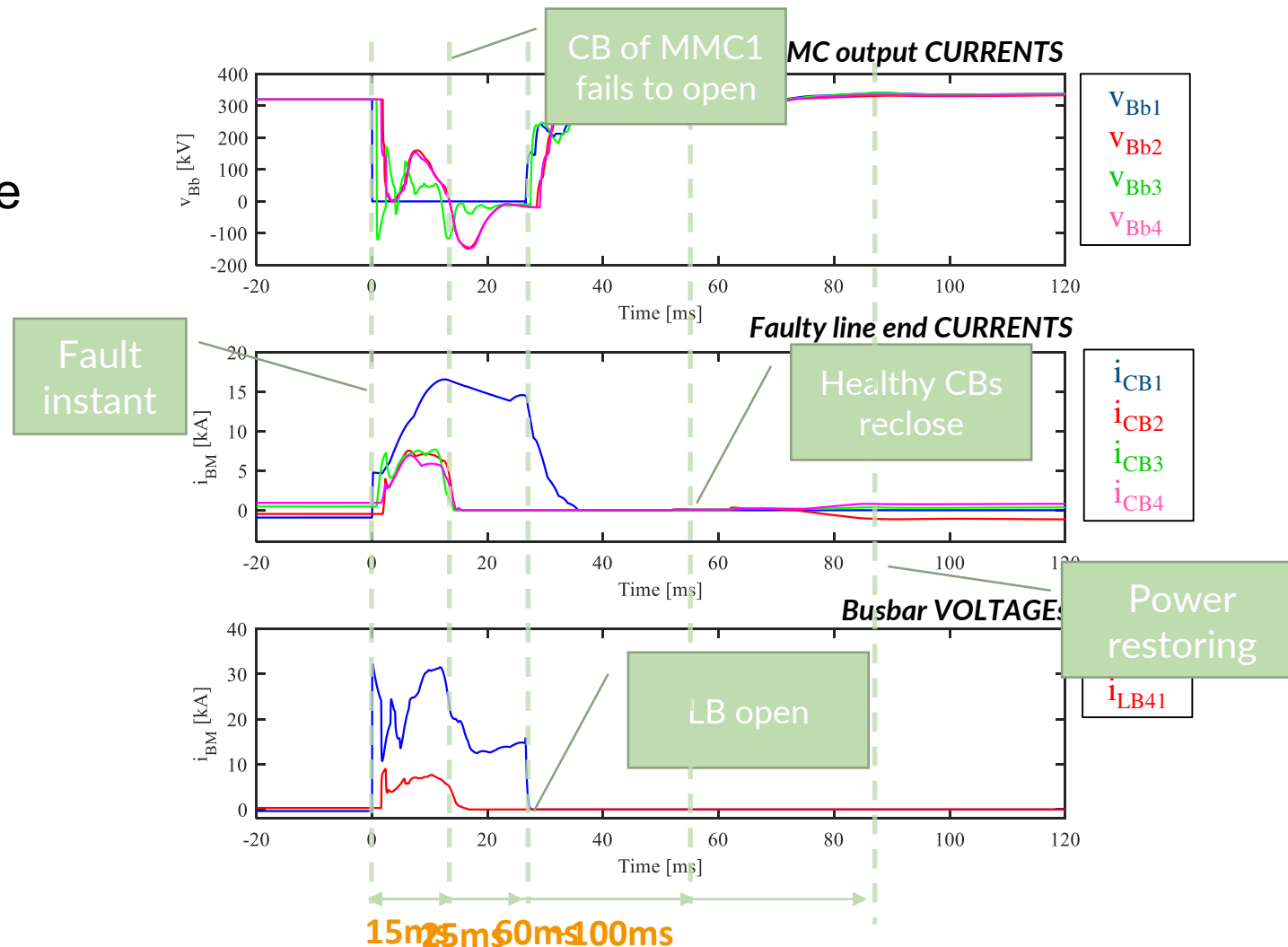
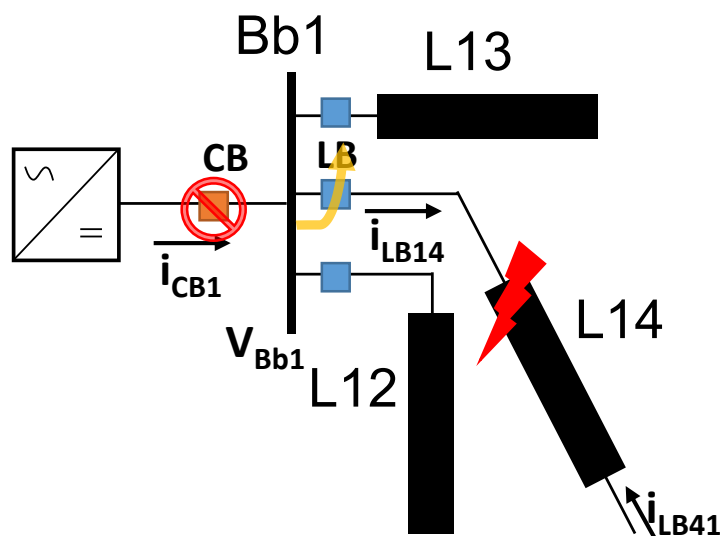
BACKUP SEQUENCES

- Case 1: Converter Breaker failure



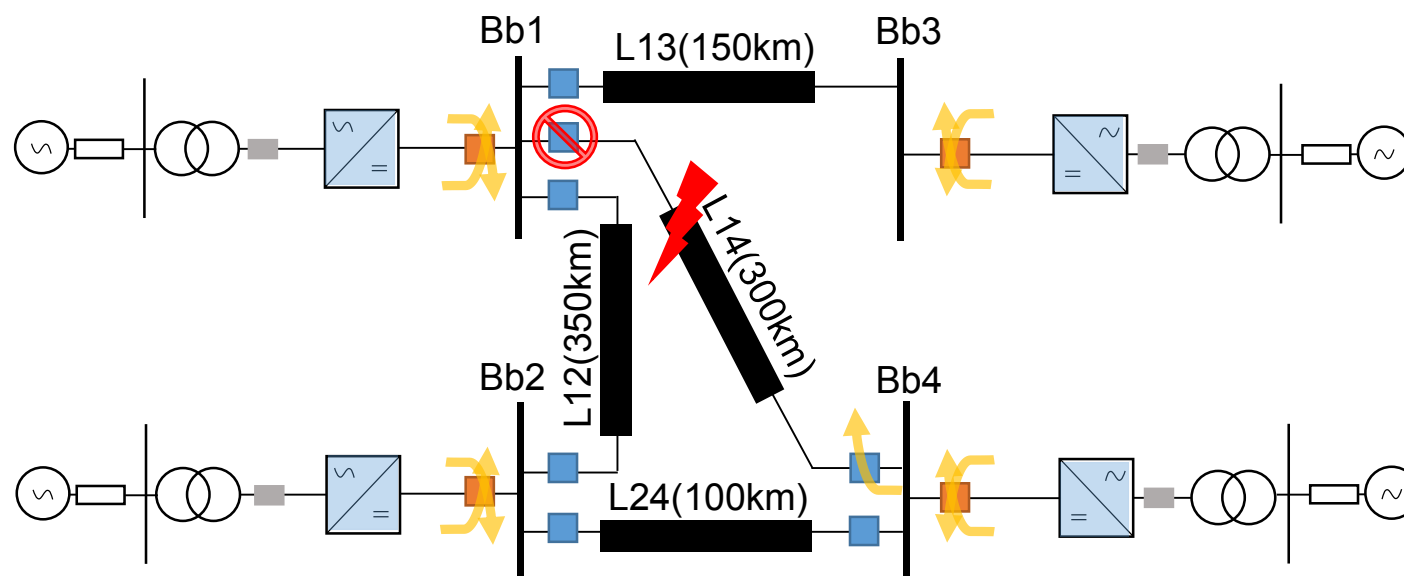
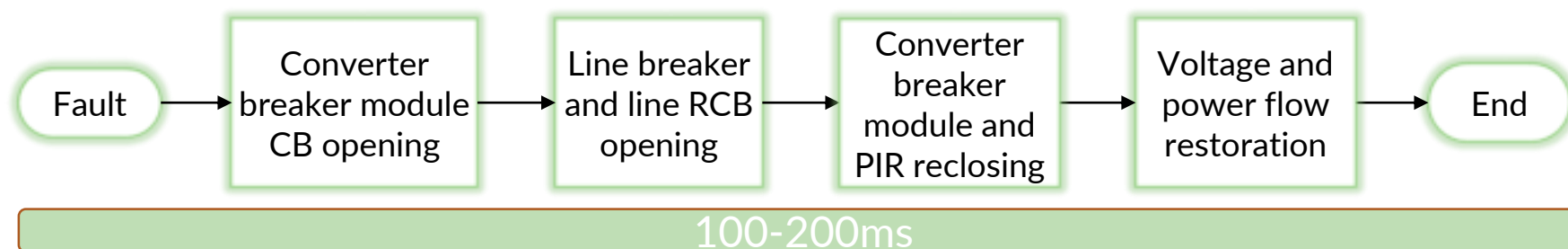
BACKUP SEQUENCES

- Case 1: Converter Breaker failure

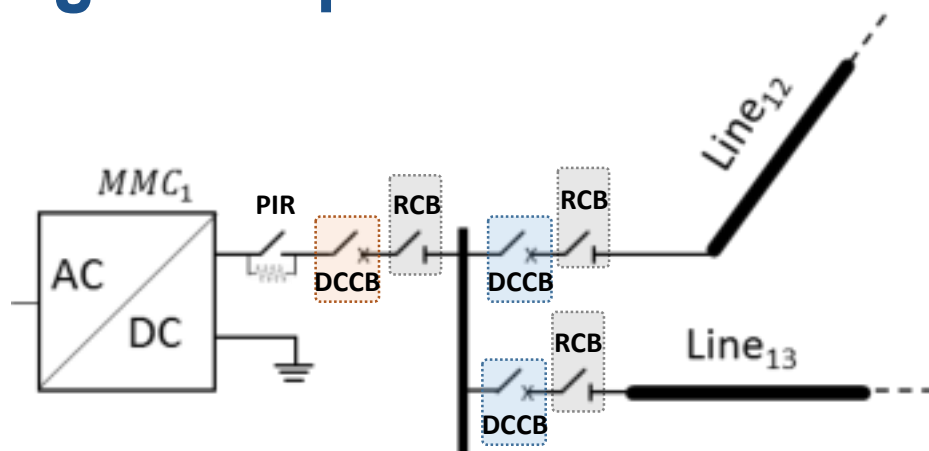


BACKUP SEQUENCES

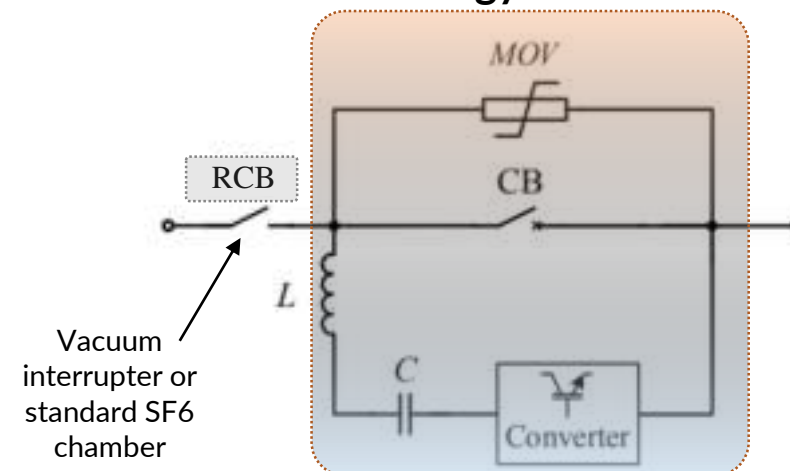
- Case 2: Line Breaker failure



Switchgear requirements



Example of possible technology for DCCB



	Converter DCCB	Line DCCB	Residual current breaker
Breaking capability	20 kA (DC)	20 kA (DC)	Few A (DC) Few kA (AC)
Breaker operation time	10-20 ms	10-20 ms	10 ms
Closing time	10-20 ms	10-20 ms	10 ms
Open-close operation	O - 50ms - CO	O	O - 50ms - CO
DC limiting reactor	Not required	Not required	/
Surge arrester energy requirement	~ 7 MJ	~ 7 MJ	/

Conclusions

- Advantages of the Converter breaker strategy
 - No need to use ultra-fast hybrid DC breaker
 - Mechanical DC breaker is a suitable solution
 - Reduced energy dissipation required within DC breaker
 - No need to use limiting inductor
 - No need to use ultra fast fault discrimination algorithms
 - Communication protocols for protection equipment can be based on IEC61850
 - MMC can work in STATCOM mode to support the AC side ~40ms after fault inception
 - Power restoring within 100-200ms for primary and backup sequences
 - No risk of transient instability when considering an AC inertia coefficient of 4 with reasonable DC power exchange
- ✓ Multivendor
 - ✓ Cost
 - ✓ Interoperability

North Sea Grid for the European New Deal

How to unlock Europe's Offshore Wind potential – a deployment plan for meshed HVDC grid



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EXPERIENCE

- Team Leader DC Systems @ RWTH Aachen since 2019
- Research Associate @ RWTH Aachen since 2016
- M.Sc. Electrical Engineering @ RWTH Aachen in 2015

PROJECT ROLE

- Work package lead of WP16
- Model development in WP2
- Development a DC grid protection strategy based on fault-blocking converters in WP2/WP4

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EXPERIENCE

- Research Associate @ RWTH Aachen since 2018
- M.Sc. Electrical Engineering @ RWTH Aachen in 2018

PROJECT ROLE

- Development of MATLAB/Simulink® and Hypersim® Models in WP9
- Research on DC grid protection based on fault-blocking converters in WP2/WP4/WP16



FULL-BRIDGE MMC BASED STRATEGY



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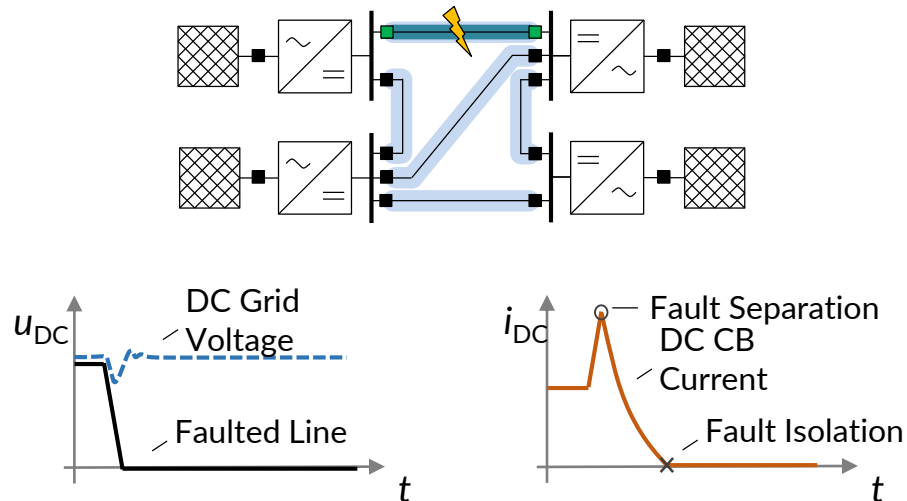


Philipp Ruffing

HVDC Grid Protection Philosophies

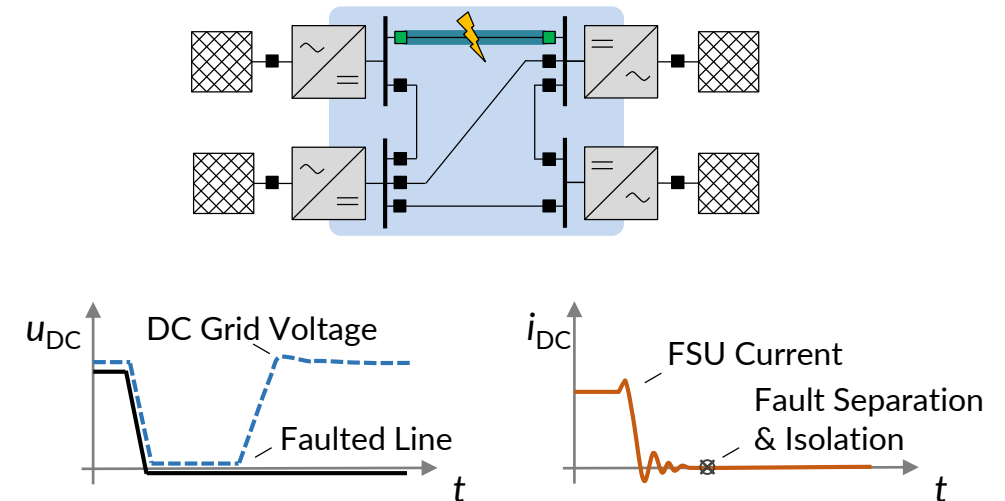
Fully Selective Protection

- Every DC line as an individual protection zone
- Fault separation by fast DC circuit breakers
- High requirements on DC switchgear



Non-Selective Protection

- Entire DC network as protection zone
- Fast de-energisation of the protection zone
- Fault separation at near-zero current and voltage



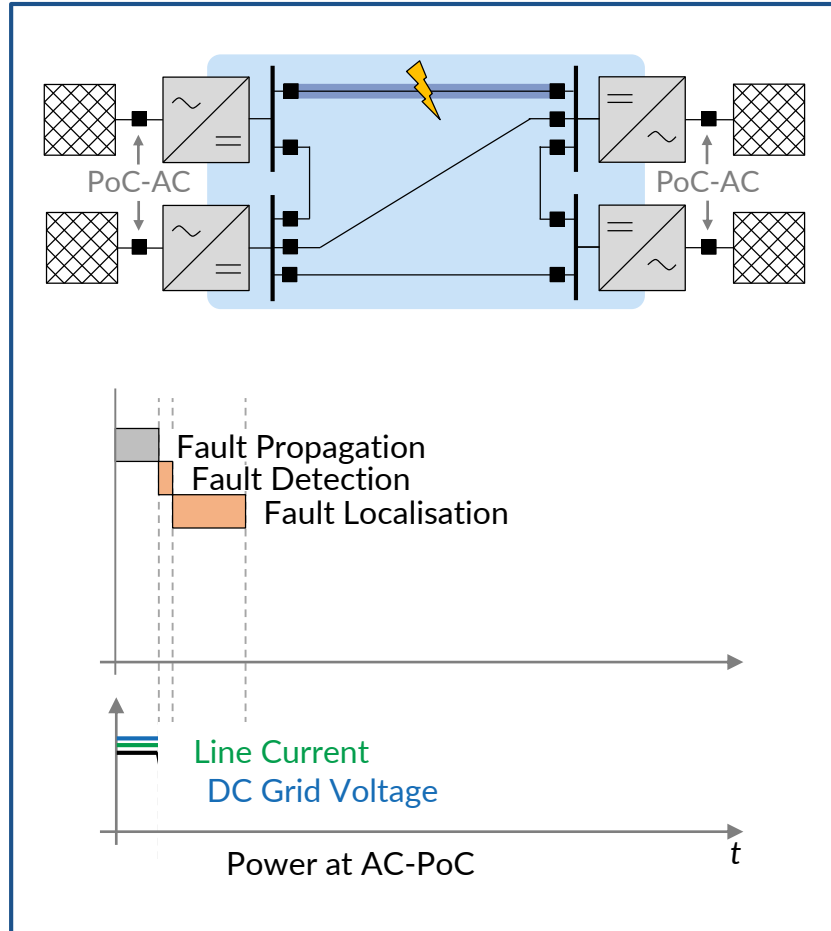
Protection Zones

Faulted Line

Fault Feeding Converter (i.e. Half-Bridge MMC)

Fault Blocking Converter (i.e. Full-Bridge MMC)

Protection Strategy – Detection and Localisation



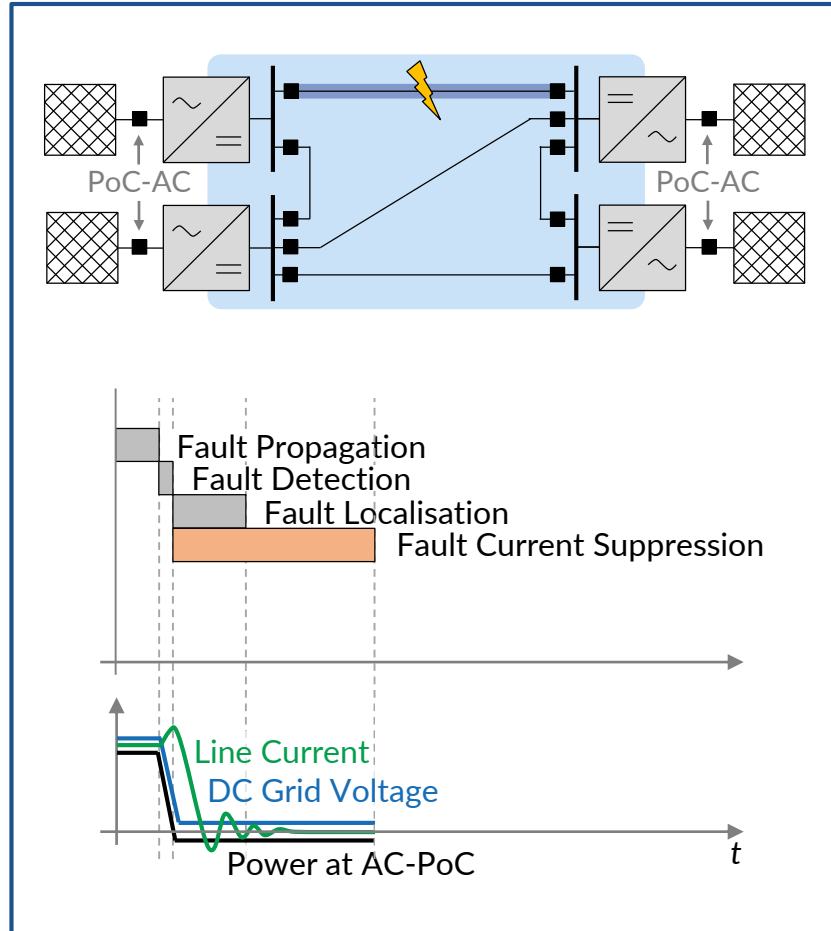
• Fault Detection

- Fault detection by every converter within the network
- Initiate the fault current suppression of each converter within the protection zone
- High-speed fault detection

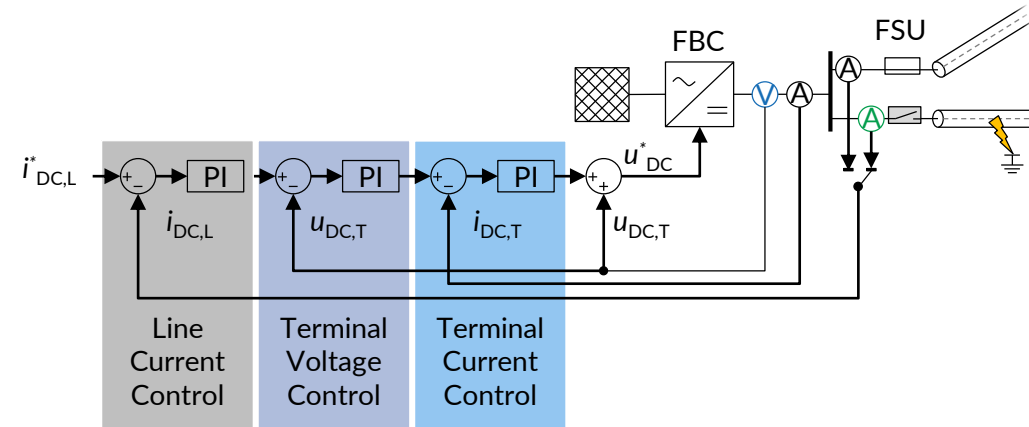
• Fault Localisation

- Localization of the line to be separated
- Required for the fault separation after the de-energization of the network
- Low-speed fault localization based on communication is sufficient for the protection strategy

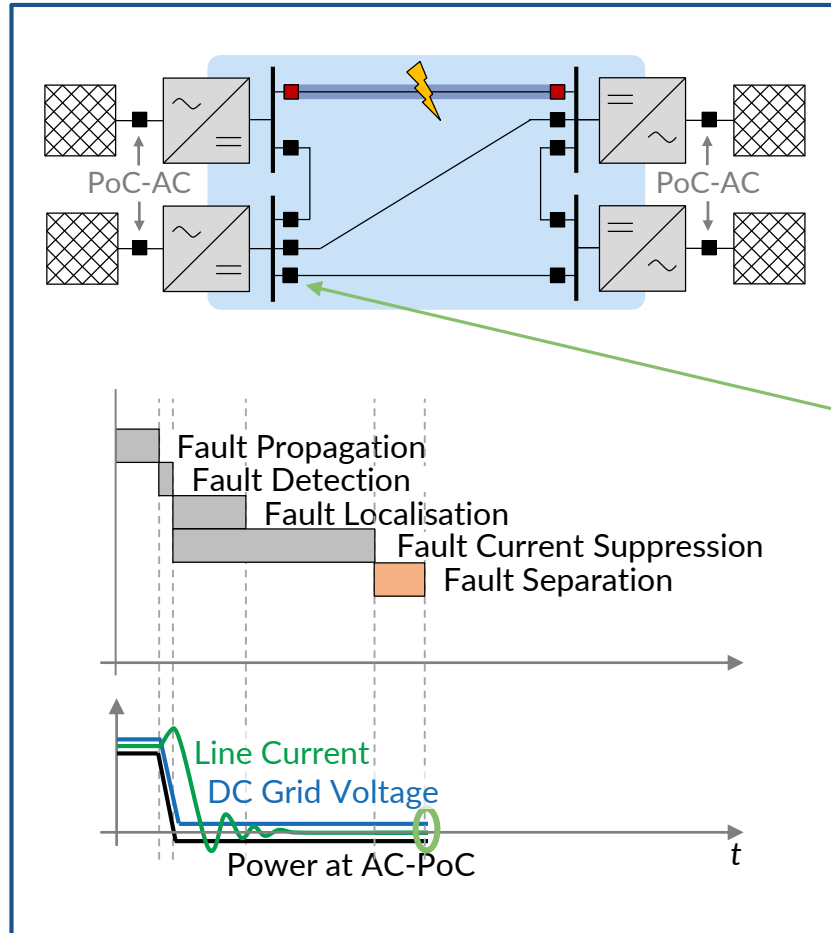
Protection Strategy – DC Fault Control



- Fast reduction of the energy injected into the DC system
 - Enable a fast fault separation under near-zero current and voltage conditions
 - Discharge the DC network
 - Reduce the current flowing through the fault separation units
- Cascaded fault control approach

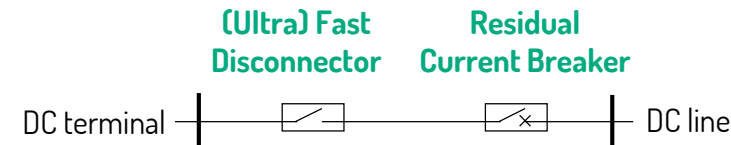


Protection Strategy – Fault Separation Unit



• Requirements

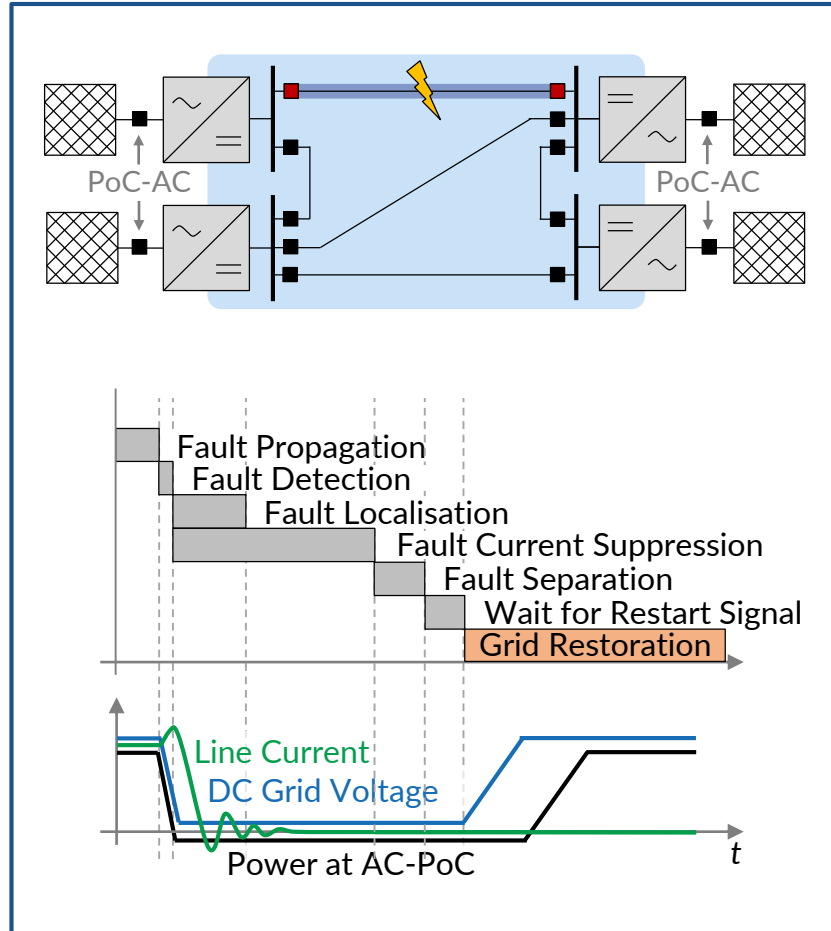
- Residual (DC) current interruption capability
→ counter voltage (transient interruption voltage) may be required
- Fast isolation of the faulted line after fault separation



• Residual Current Breaker (RCB)

- Voltage ratings (TIV) ~ 5 – 10 % of V_{DC}
- Energy absorption ~ a few tens of kilojoules
- RCB can be adjusted to the power system's requirements

Protection Strategy – Grid Restoration



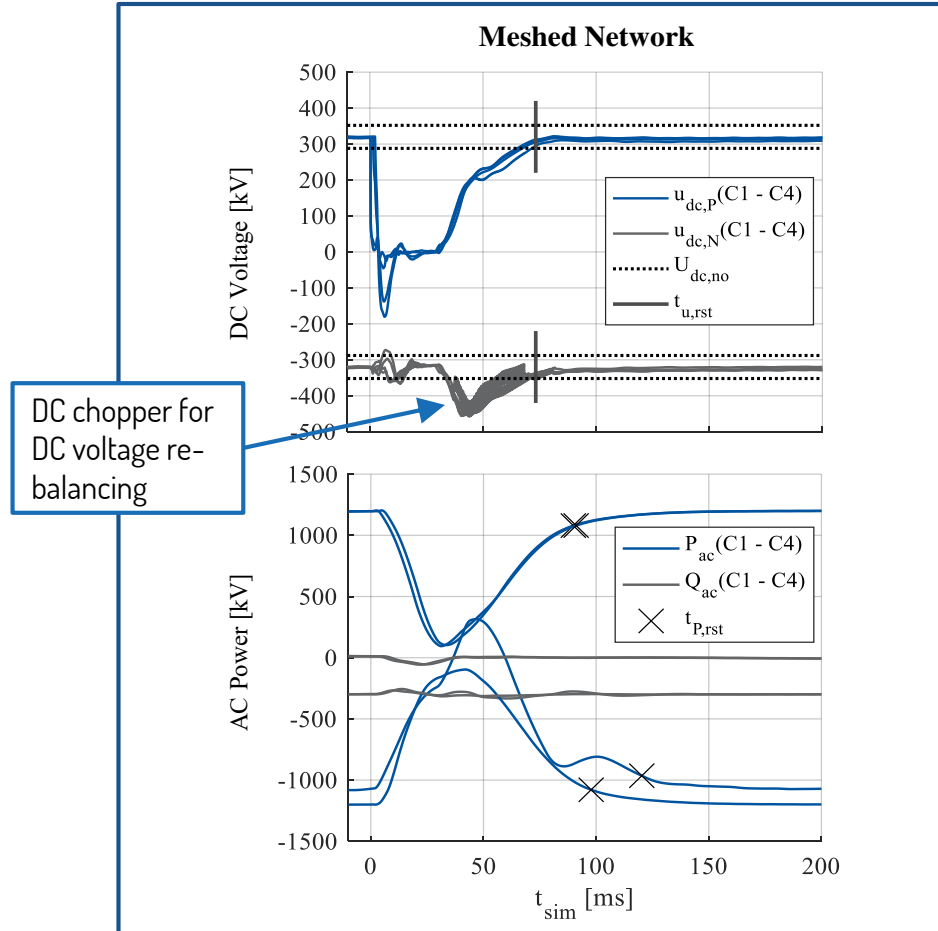
• DC Voltage Restoration

- Symmetrical monopole configuration
 - Pole-voltage rebalancing required
 - By: DC choppers, AC-side zero-sequence grounding or converter-controlled rebalancing
- Bipole configuration
 - No pole-voltage rebalancing required

• Active Power Restoration

- Fast active power restoration since no line inductors are required for the protection strategy

Protection Strategy – Performance



- Key Performance Indicators (4-terminal HVDC network):
 - Fault Separation Time: 20 – 50 ms
 - DC Voltage Restoration Time: 50 – 100 ms
 - Active Power Restoration Time: 70 – 150 ms
 - Transient Energy Imbalance: 20 – 70 MJ
 - Reactive Power: No outage, since MMCs are continuously controlled
- FBC-based protections systems can be competitive alternative to DC circuit breaker based HVDC grid protection systems for “small” networks

SCOPE OF THE HARDWARE-IN-THE-LOOP DEMONSTRATION



William Leon-
Garcia



Antoine
Ghyselinck



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How to unlock Europe's Offshore Wind potential – a deployment plan for meshed HVDC grid



William LEON GARCIA

Research engineer

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• EXPERIENCE

- PhD in electrical engineering research on HVDC grid protection and applied superconductivity
- 3-years in HIL testing, real-time simulation and prototyping at SuperGrid Institute

• PROJECT ROLE

- **Technical leader of tasks T9.7 and T9.8 in WP9:**
Demonstration of non-selective fault clearing strategies for meshed HVDC networks



William
Leon Garcia

SCOPE OF THE DEMONSTRATION

System layout



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OVERVIEW

Demonstration of two kinds of non-selective protection strategies

Converter Breaker Protection Strategy (CBS)



Bipole

Half Bridge MMC

Converter Breaker

Mechanical DC Circuit Breakers

Full Bridge converter based protection Strategy (FBS)



RWTH AACHEN
UNIVERSITY

Asymmetric Monopole

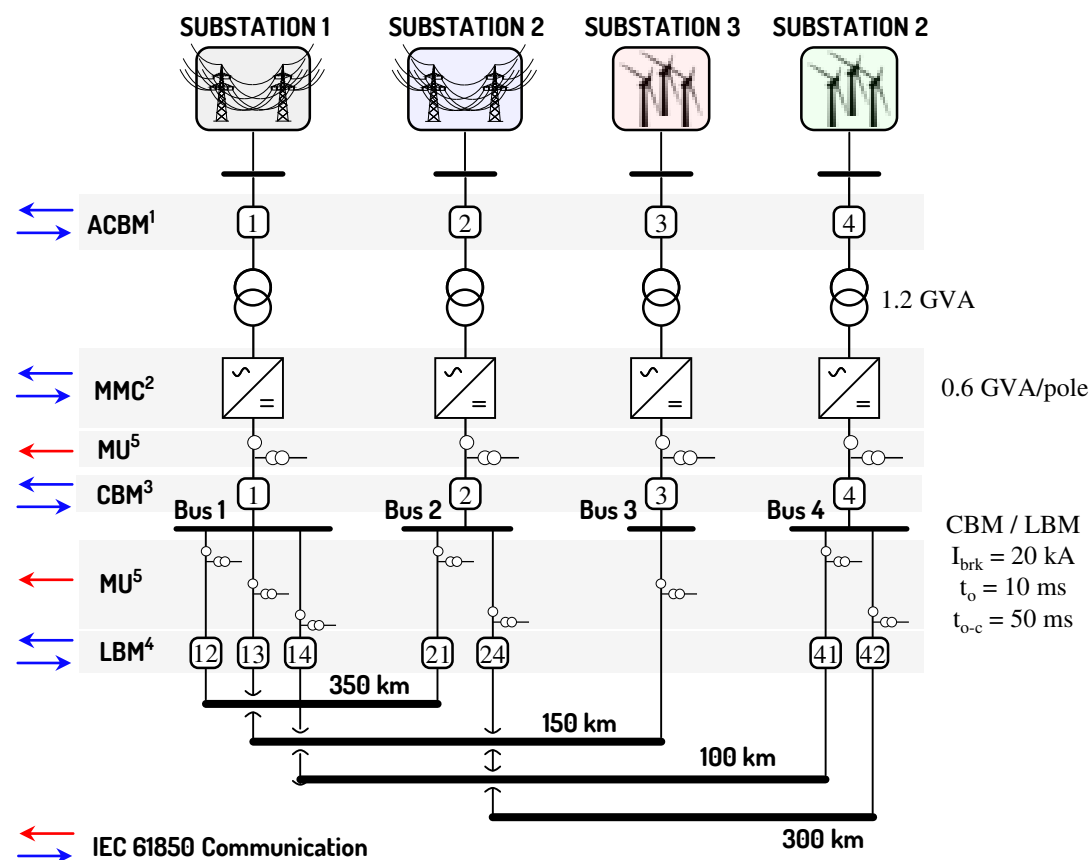
Full Bridge MMC

Fault current control

High Speed Switch

PLANT – CONVERTER BREAKER PROTECTION STRATEGY

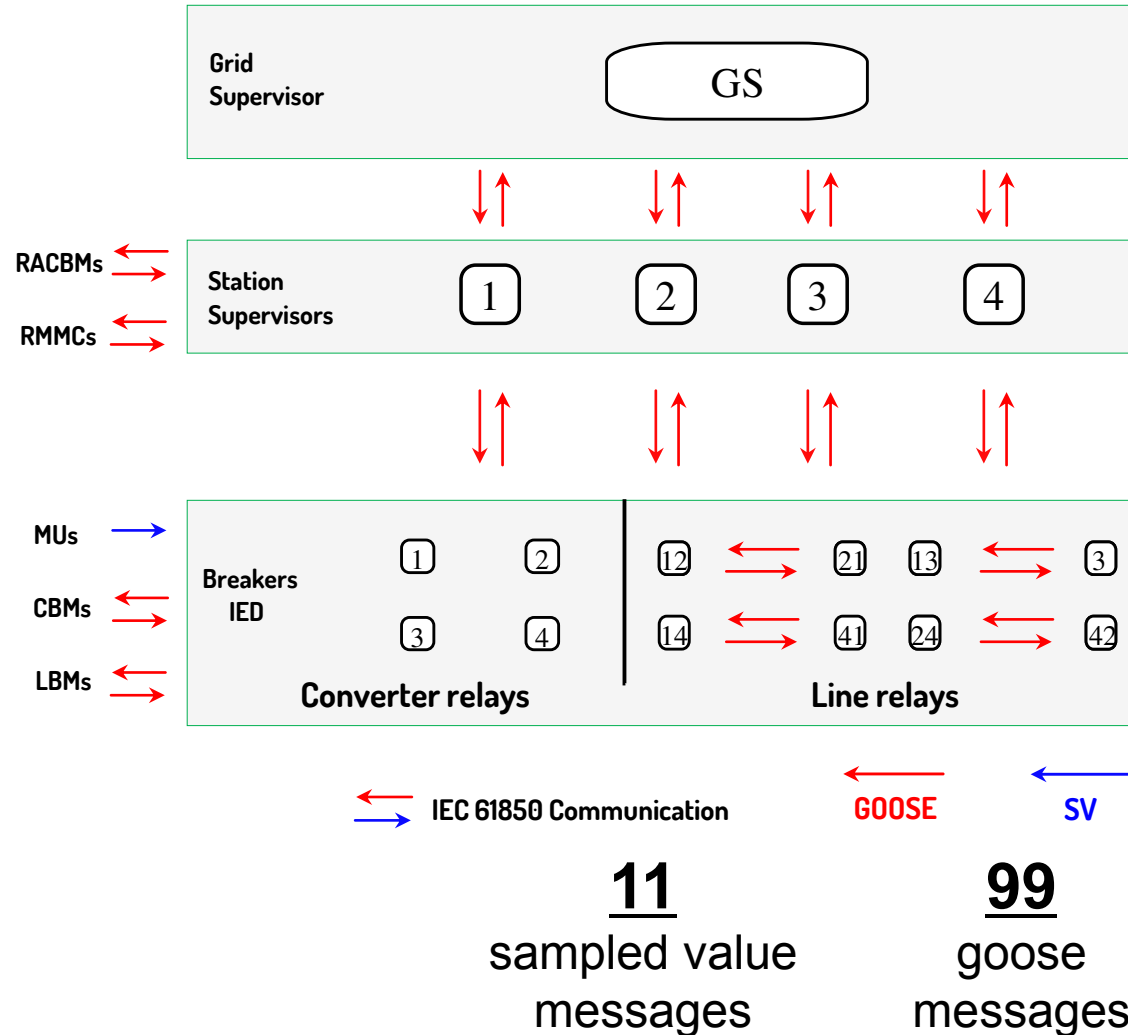
Four-terminal meshed HVDC network



- Bipole (one pole represented)
- A lot of communication is needed
- One pole simulated
 - Lighter for :
 - The simulation target
 - The ethernet network (one switch)

¹AC breaker module
²Modular multi-level converter
³Converter breaker module
⁴Line breaker module
⁵Merging Unit

DEVICES UNDER TEST – CONVERTER BREAKER PROTECTION STRATEGY - Communication architecture



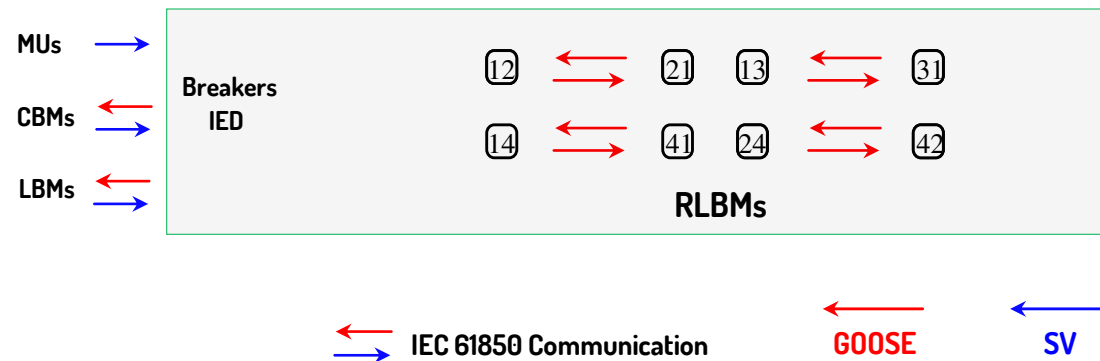
- 4 layers of communication :
 - Network <-> Relays
 - Relay <-> Relay
 - Relays <-> Station Supervisors
 - Station Supervisors <-> Grid Supervisor
- RLBM on the same line communicate to give current direction information.

[illegible]

- Asymmetric monopole
- The full-bridge converter has fault current controlling capability
 - Converter breaker not needed
 - Line breaker module:
 - Residual current breaker +
 - High speed switches
- Model can startup without supervision, and supervision is not needed by protection

- ¹AC breaker module
- ²Modular multi-level converter
- ³Line breaker module
- ⁴Merging Unit

DEVICES UNDER TEST – FULL BRIDGE CONVERTER PROTECTION STRATEGY - Communication Architecture



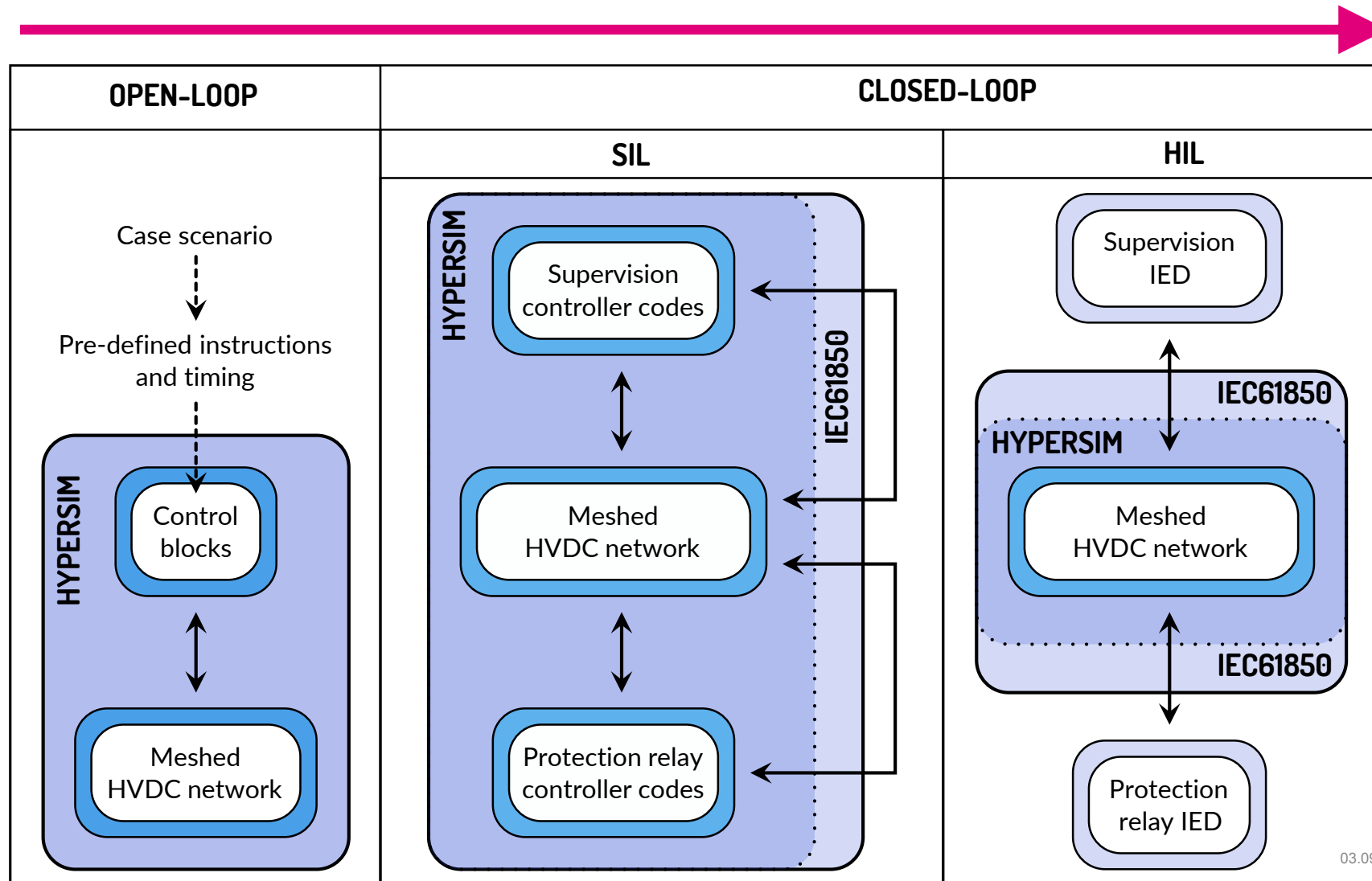
- Full-bridge converter supervision included in simulation model
 - Communication simplified: less signals and layers.
- 2 layers of communication :
 - Network <-> Relays
 - Relay <-> Relay
- RLBM on the same line communicate to exchange current direction information.

8
sampled value
messages

43
goose
messages

HARDWARE-IN-THE-LOOP

Demonstration workflow



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Research engineer

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• EXPERIENCE

- Engineer degree in power systems
- Internship on AC/DC grid stability
- 1 year on HIL testing and real-time simulation at Supergrid Institute

• PROJECT ROLE

- Implementation of the Demonstration of non-selective fault clearing strategies for meshed HVDC networks



SCOPE OF THE DEMONSTRATION

Hardware-in-the-loop setup

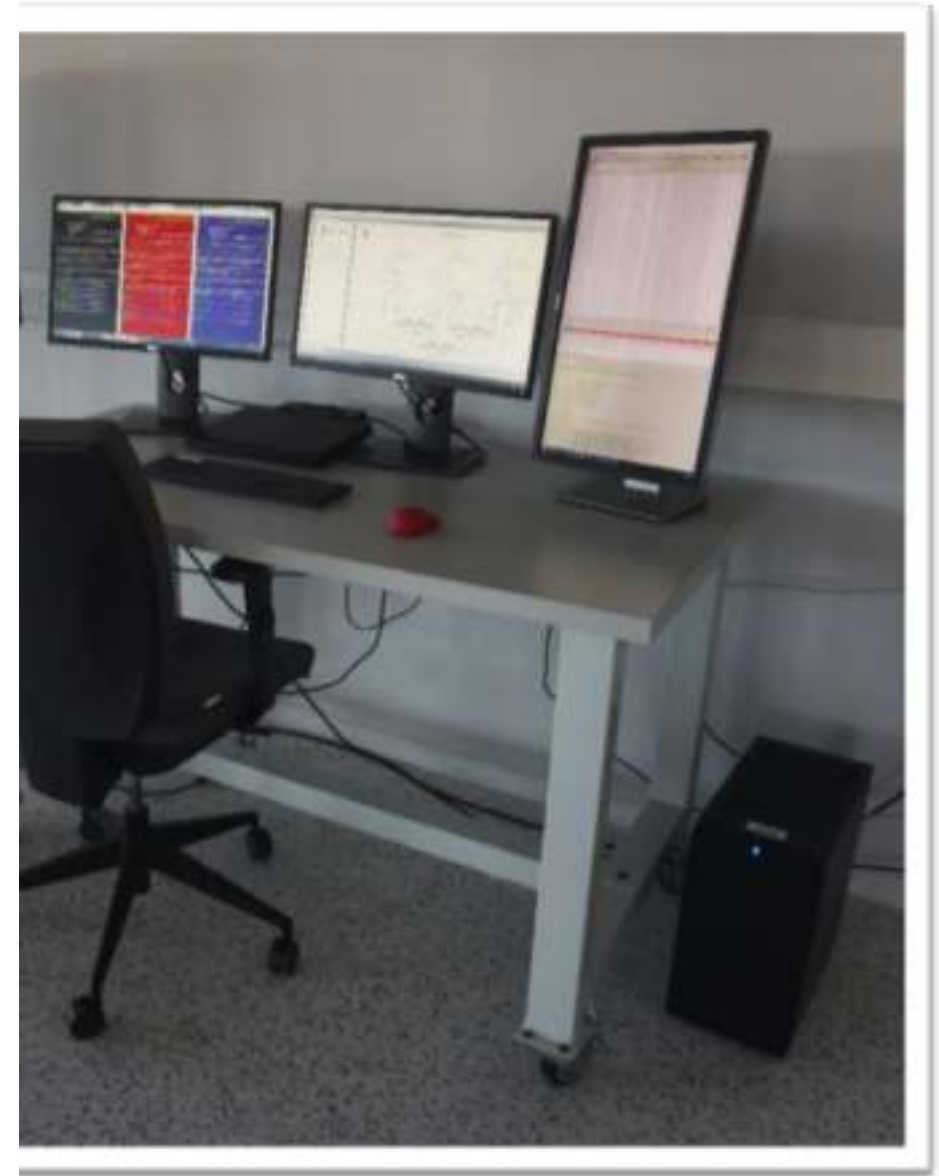


Antoine
Ghyselinck



USER'S WORKSPACE

- Good grade desktop PC with all the softwares needed for HIL set up.
- Several monitors to display results from the different softwares.



SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup



SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup



Opal-RT OP5700 Target

Items	Quantity	Description
Operating System	1	Redhat v2.6.29.6-opalrt-6.1
Chassis Type	1	OP5700
CPU	2	Intel Xeon E5, 8Cores, 3.2 GHz, 20M Cache
Total Core *	16	
Memory	4	8 GB
Motherboard		X10DRL-I Supermicro Motherboard Dual Intel® Xeon® (E5) processor
IP Address		192.168.10.101 (eth 0) - PF616171S01 192.168.10.103 (eth 0) - PF616171S03 - see Figure 1 for Ethernet port identifications
AC Input		115-230V, 60-50Hz
FPGA Board Index		00

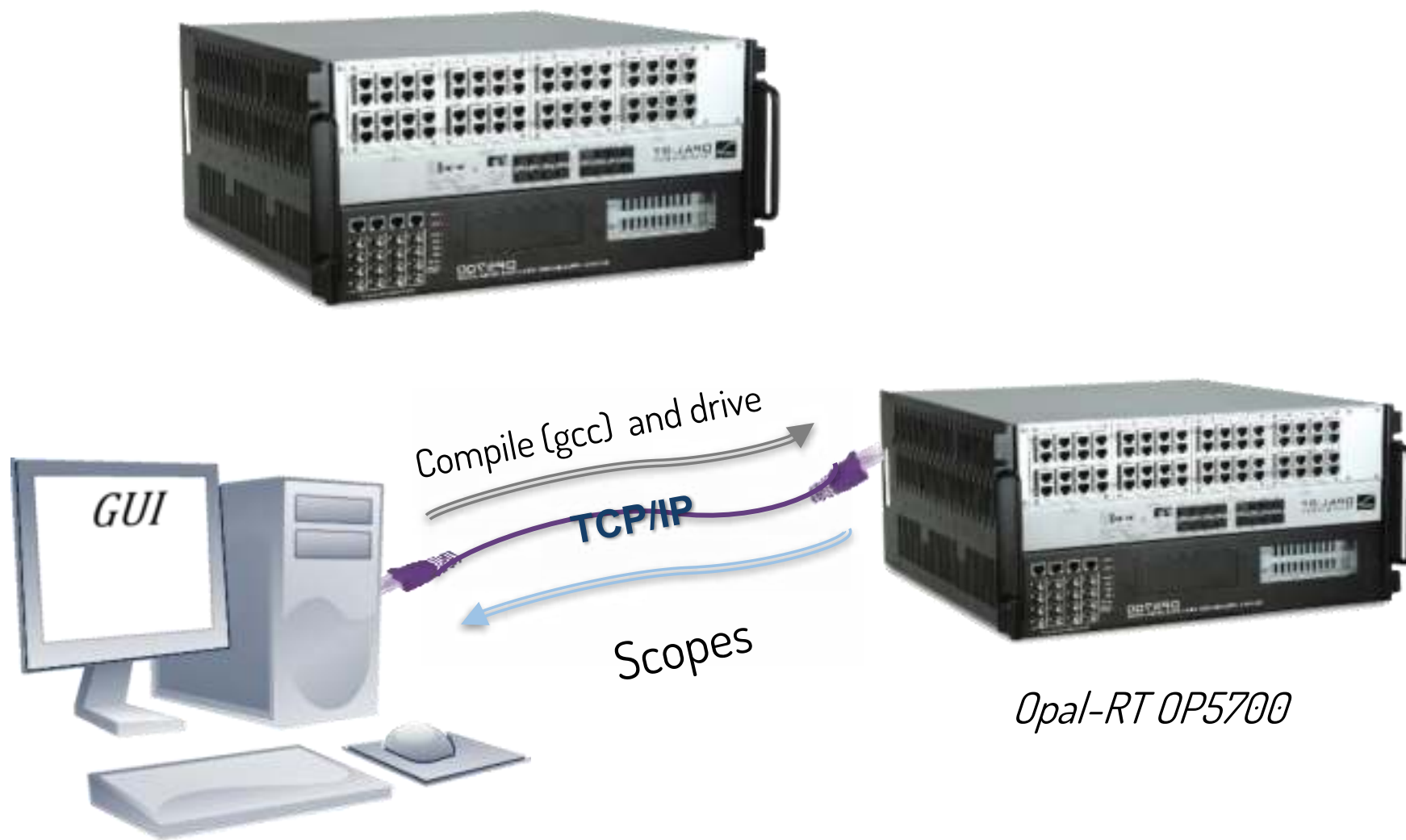
*Our license can run up to 10 cores on a simulation

OPAL-RT OP5700 Target Hardware

Id	Exec	Exec Max	Sim	Sim Max	IO Out Max	IO In Max	Last in Sync	Stretched Step
1	16.76	40.0	49.99	50.66	0.06	0.08	109428	0
2	1.57	2.51	46.71	60.65	0.61	13.72	0	0
3	1.25	2.0	44.06	65.35	9.07	13.0	0	0
4	1.98	5.5	47.7	59.69	0.11	13.81	0	0
5	4.17	5.12	46.99	66.28	11.43	12.21	19	0
6	1.82	4.97	49.96	60.85	0.06	13.61	0	0
7	1.98	6.62	52.66	59.73	0.6	13.86	0	0
8	5.17	12.3	53.96	62.06	0.18	14.43	0	0
9	10.55	19.0	50.03	51.06	0.26	0.44	0	0
10	6.94	18.81	50.01	50.92	0.32	0.47	0	0

Hyperview during a simulation (Target Analyzer)

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup



SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

INTELLIGENT ELECTRONIC DEVICES



Rack of 20 RPI

CBS : 11 Relays, 5 Supervisors

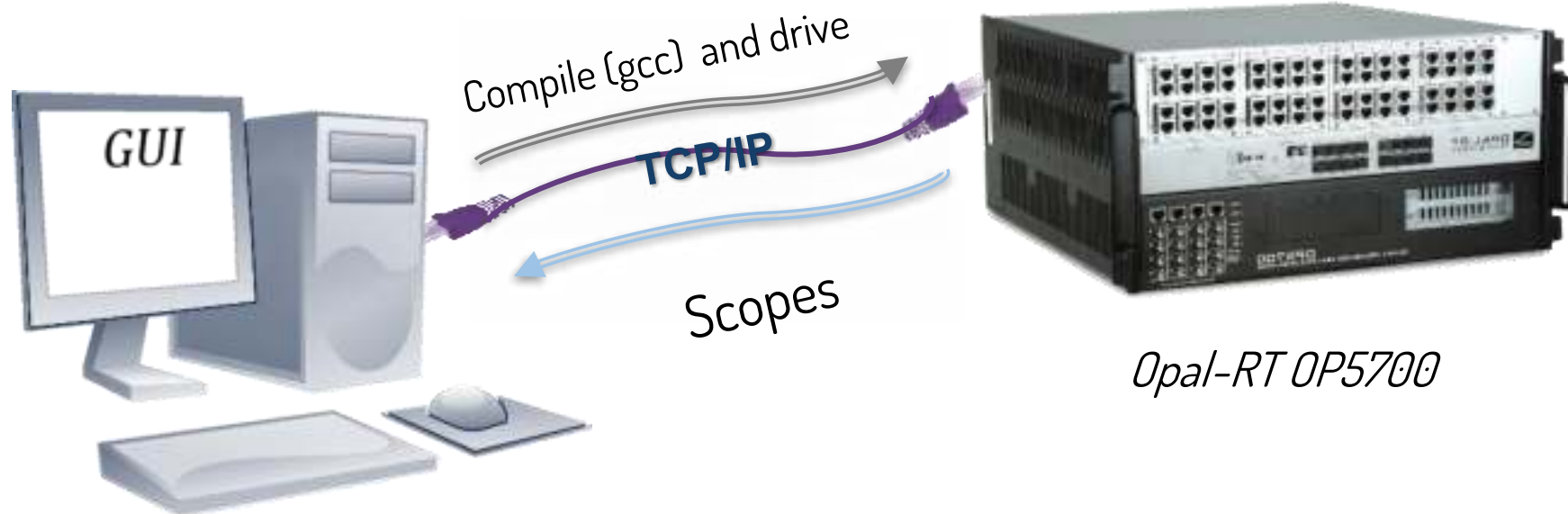
FBS : 8 Relays



System on Chip	64-bit quad-core Cortex-A72 processor
Clock speed	1.5 GHz
RAM	4GB LPDDR4 SDRAM
Communication	Native Gigabit Ethernet port
Operating System	Debian
Dev tools	Text editor, gcc (compiler) , gdb (debugger)

Raspberry PI 4B Overview

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

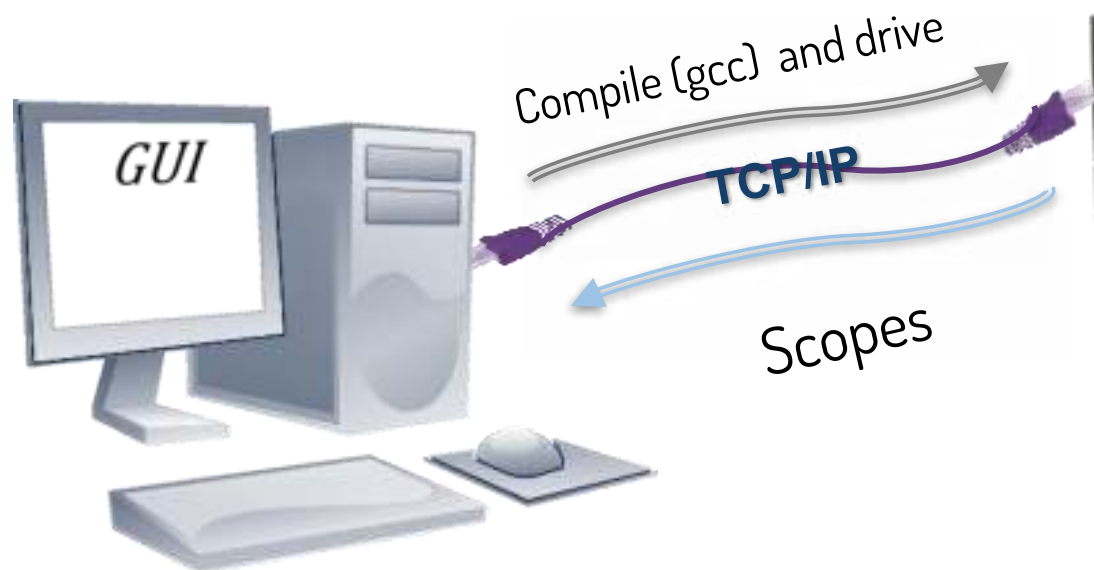
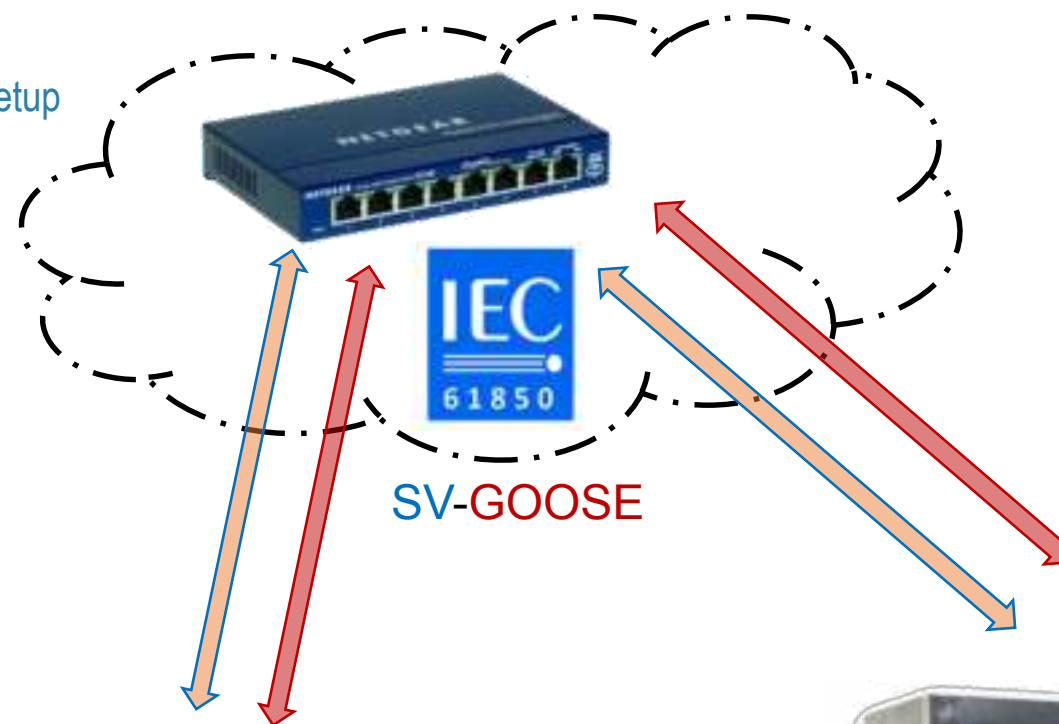


Opal-RT OP5700



Rack of RaspberryPi 4

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

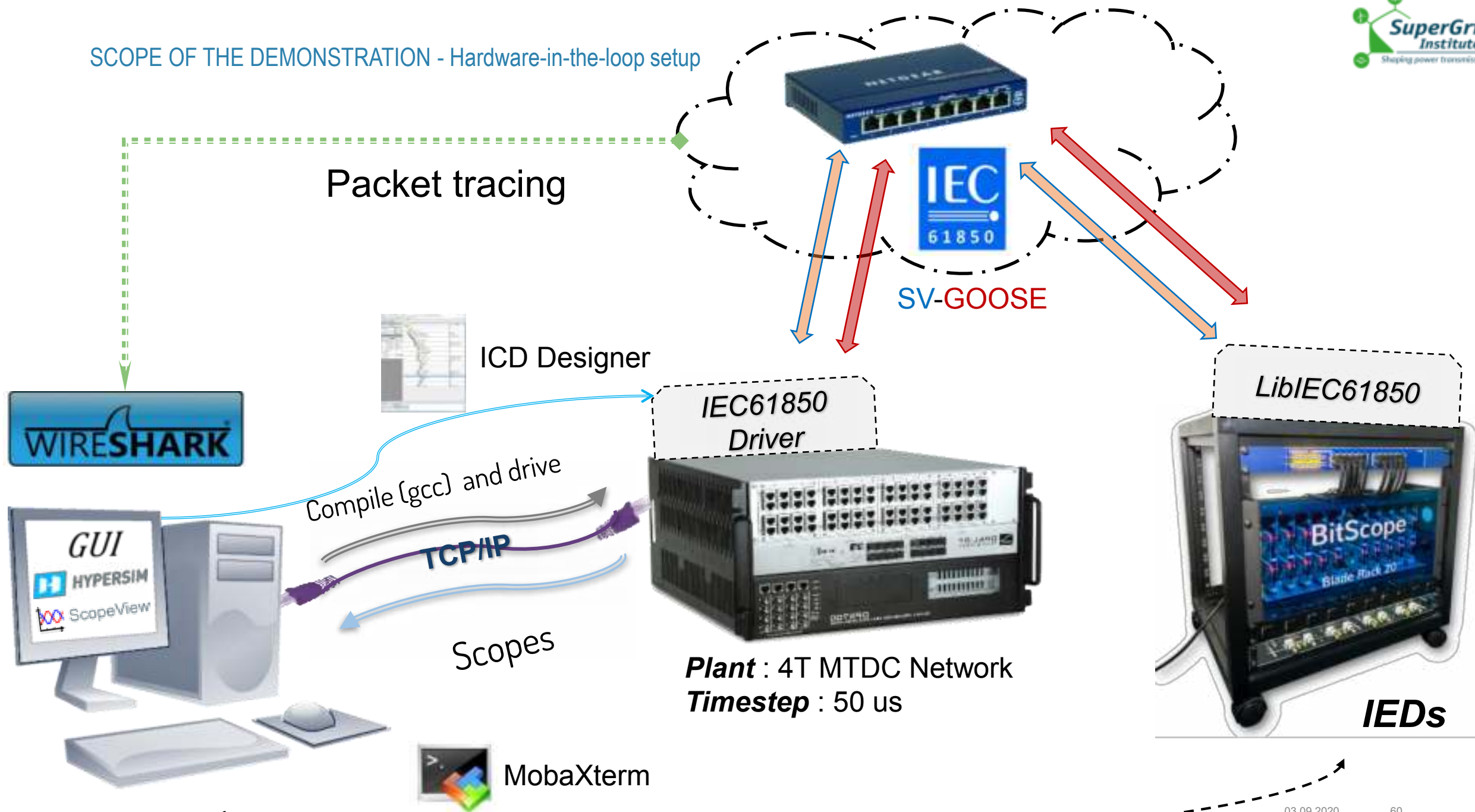


Opal-RT OP5700










Rack of RaspberryPi 4

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup



THE BIG STEPS

		<i>CBS</i>	<i>FBS</i>
Build HYPERSIM models		X	
Collaboration with RWTH for model and algorithms			X
Real time implementation and validation		X	X
Implement protection relays		X	X
Implement supervisors		X	
IED prototype development		X	X
Set up communication with IEC61850		X	X



William Leon-Garcia

SCOPE OF THE DEMONSTRATION

Real-time simulation models



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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

BUILD HYPERSIM MODELS

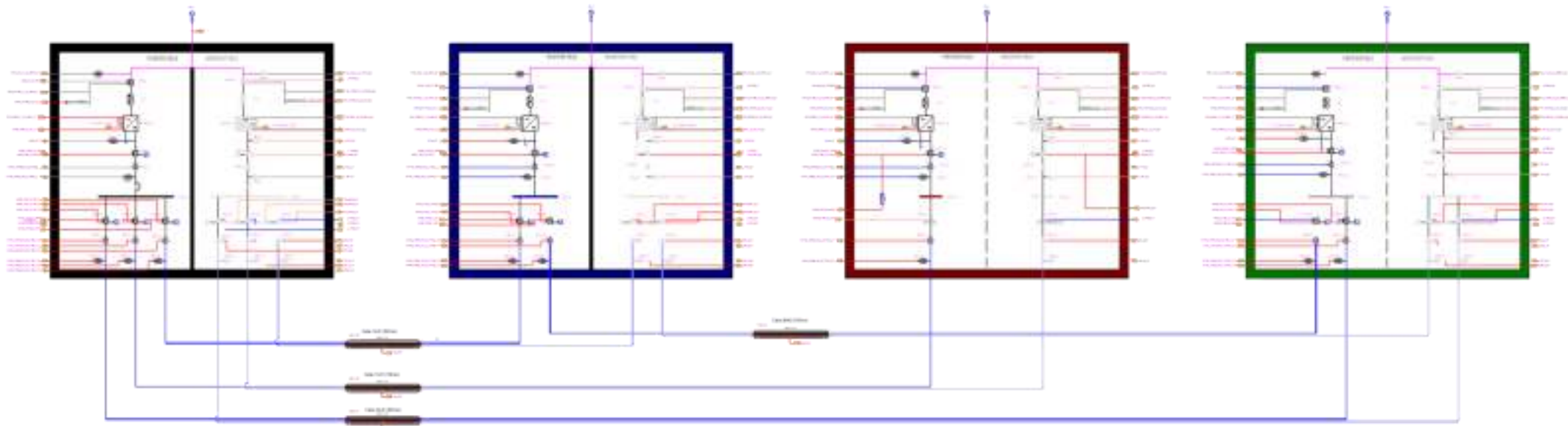


Four-terminals meshed HVDC network for CBS protection strategy

- Real-time models developed in other PROMOTioN workpackages are compatible with RTDS.
 - We needed to built them from scratch for OPAL-RT solutions.
- Main models required : MMC , DC Breakers, Cable
 - These models were created based on documents from other workpackages' and know-how in modeling of HVDC technologies.

1056
network
elements

2167
control
blocks



BUILD HYPERSIM MODELS

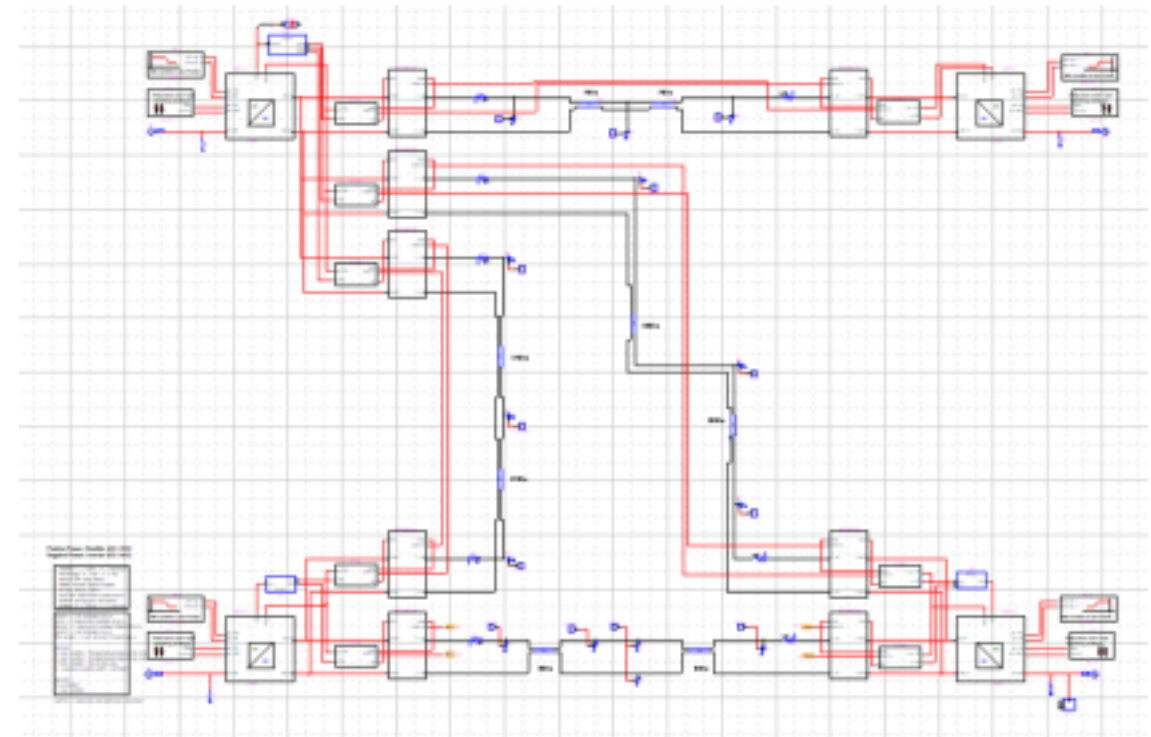


Four-terminals meshed HVDC network for FBS protection strategy

- The model was given by RWTH with a full documentation (☺)
 - Depth Understanding of the FBS (literature, documentation, collaboration with RWTH)
 - Handling of the model
- Real time implementation tasks:
 - Task managing
 - Decoupling if necessary

1251
network
elements

1851
control
blocks

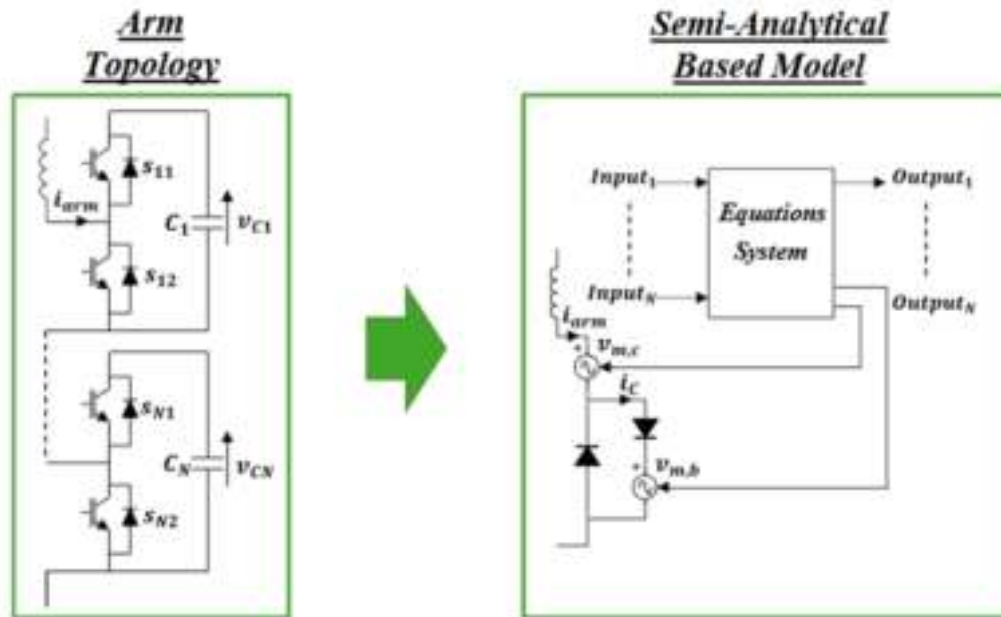


BUILD HYPERSIM MODELS

Semi-analytical average model of Modular Multilevel Converter

Physical Model

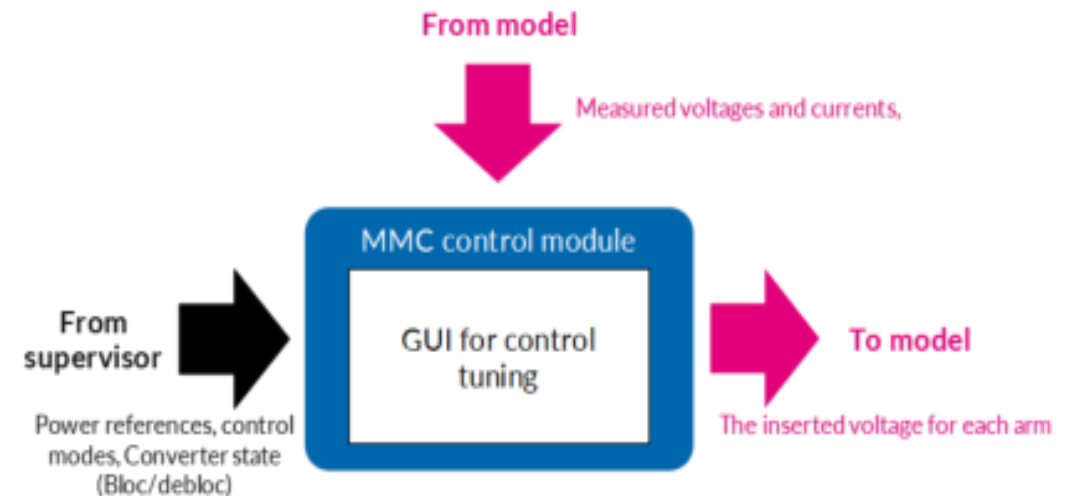
- i.e. Average Model based on the HB Valve in the HYPERSIM library.



Average Model reduction of the MMC's arm

Control

- HB-MMC control (ZAMA Ahmed, SuperGrid Institute) in Simulink imported in HYPERSIM via Hyperlink.
- FB-MMC control (RUFFING P, DÜLLMANN P)



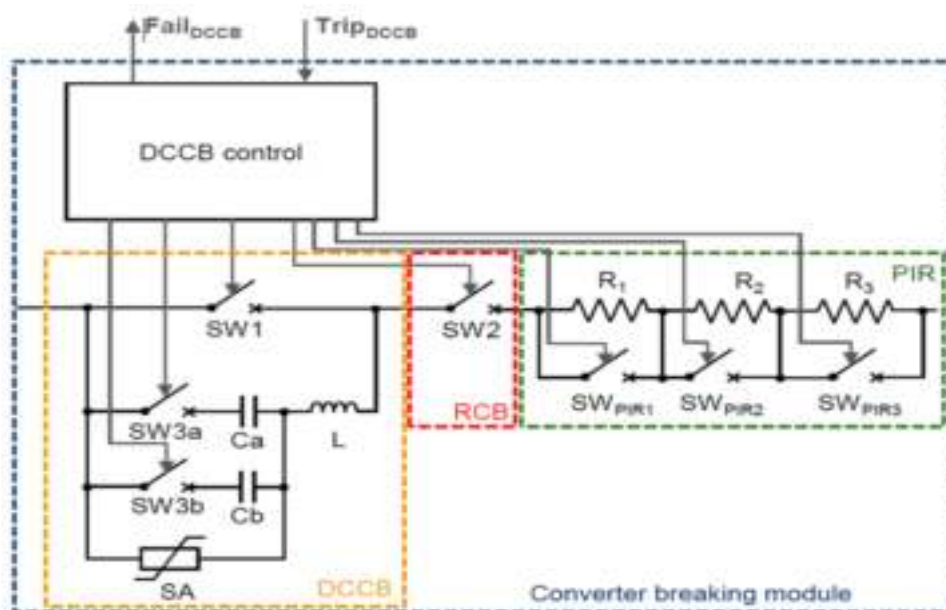
MMC Control Integration

BUILD HYPERSIM MODELS

DC circuit breakers

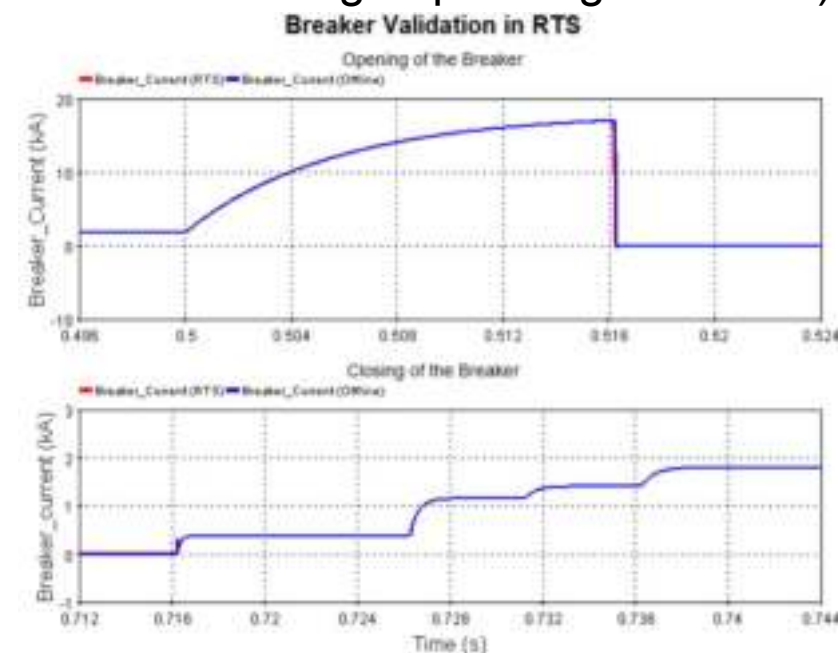
• CBS

- Active resonant DC breaker made from the WP6 literature
- Breaker model validation



FBS

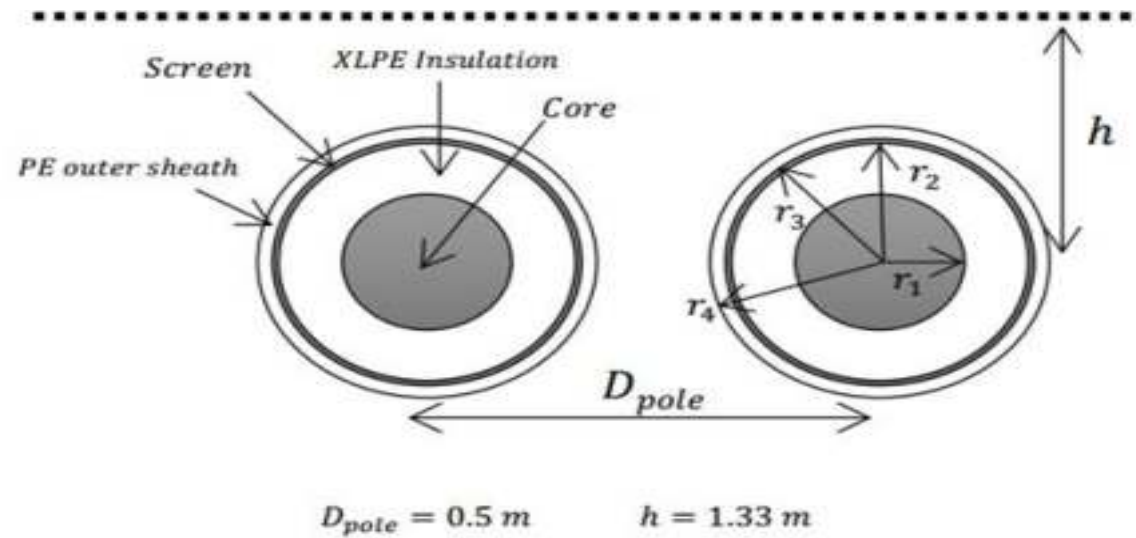
- Residual current breaker
- Ultra fast disconnecter
- Models are simplified but follow the specifications (ideal switch with adapted delays, current and voltage operating threshold)



BUILD HYPERSIM MODELS

DC Cable

- Wideband cable model



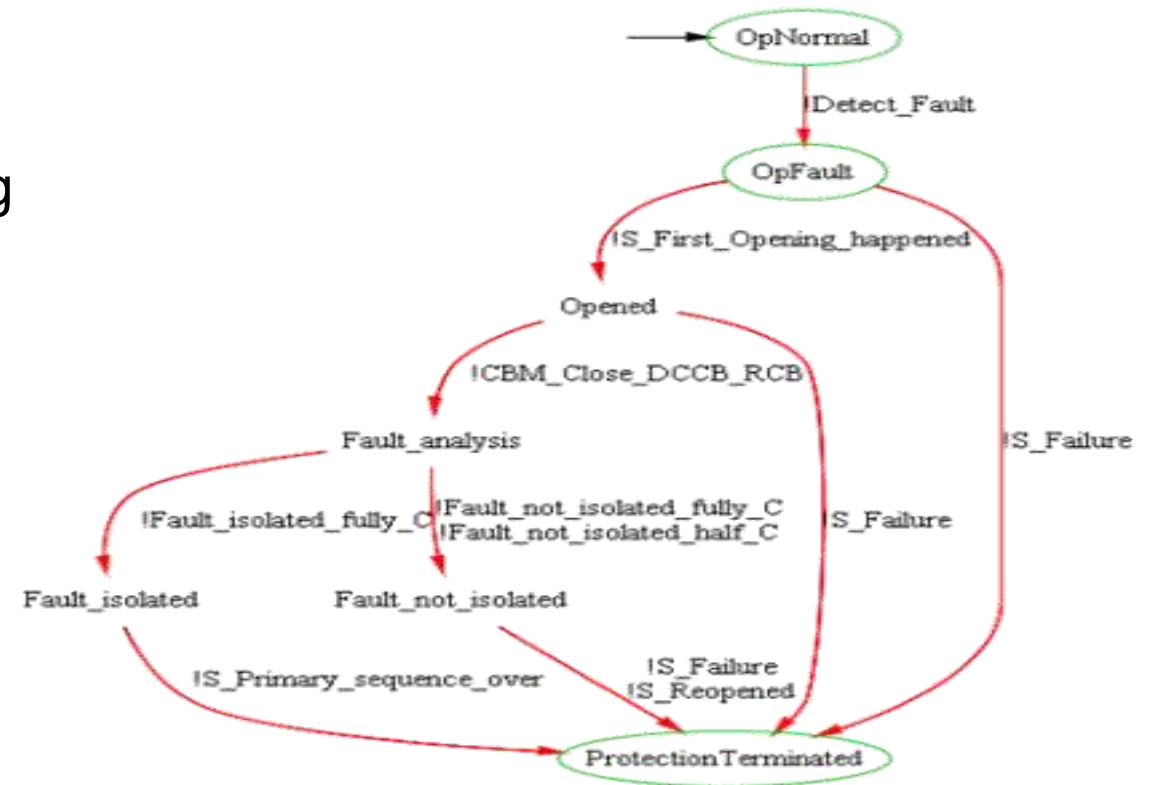
DC Cable Description

- Heavy computation, some assumptions has been made:
 - Screen grounded at both ends (limit number of sections)
 - Screen effect neglectable -> reducing number of conductors (4 to 2)

BUILD HYPERSIM MODELS

Supervisors design

- Discrete events controllers which will coordinate the associated system according to its inputs
- The associated system can be a station or the entire network
- Defined by two types of technical specifications :
 - A state diagram
 - A list of I/O
- Board to IED :
 - Extraction to C functions (SUPREMICA)



State diagram for fault supervision

SCOPE OF THE DEMONSTRATION

Hardware-in-the-loop setup



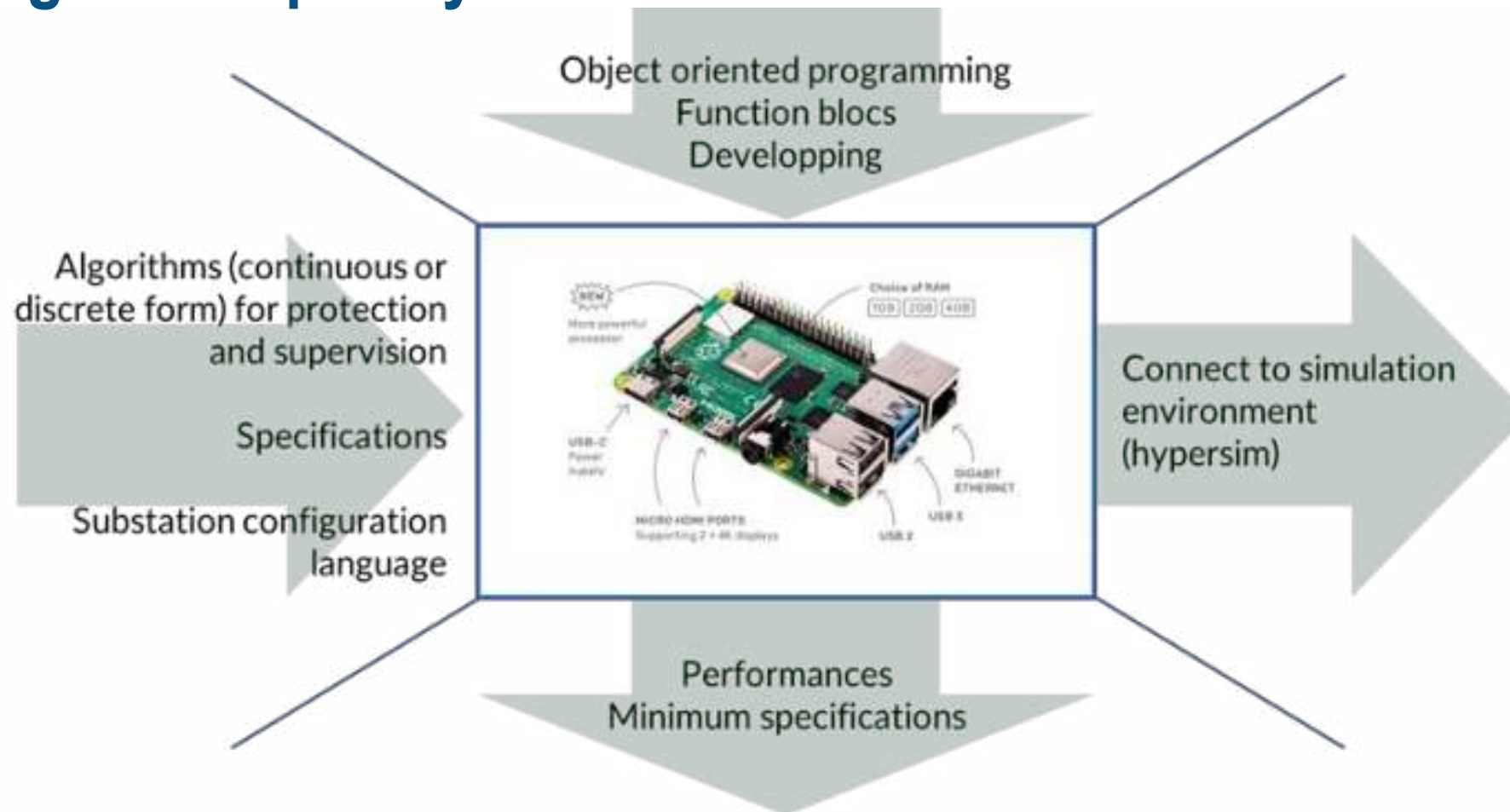
Antoine
Ghyselinck



SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

INTELLIGENT ELECTRONIC DEVICE (IED)

Prototyping on Raspberry Pi 4b



IED PROTOTYPING

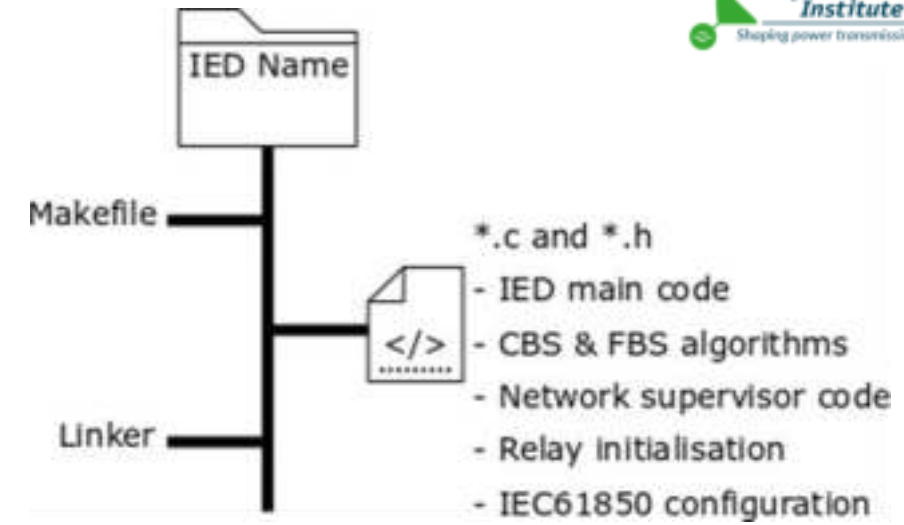
C code algorithms

- Why C code ?
 - Low level language, achieving speed requirements
 - IEC61850 Library is made for C code
- In depth C code learning required to :
 - Translate algorithms in a structured way
 - Meet the specifications



IED PROTOTYPING Structure

- Object Oriented thanks to structure
 - Relays are structures containing several attributes
 - Algorithms are C code methods designed :
 - From scratch based on specifications (ex : WP4)
 - From a third party software
- Communication managed by different C files using IEC61850 library
- In the end, the executable file is a reusable “skeleton” for our IEDs
 - Initialize relay and communications
 - Execution Loop (constant time step) :
 - Call different methods
 - Publish results



IED PROTOTYPING



Full-bridge converter based protection algorithms implementation

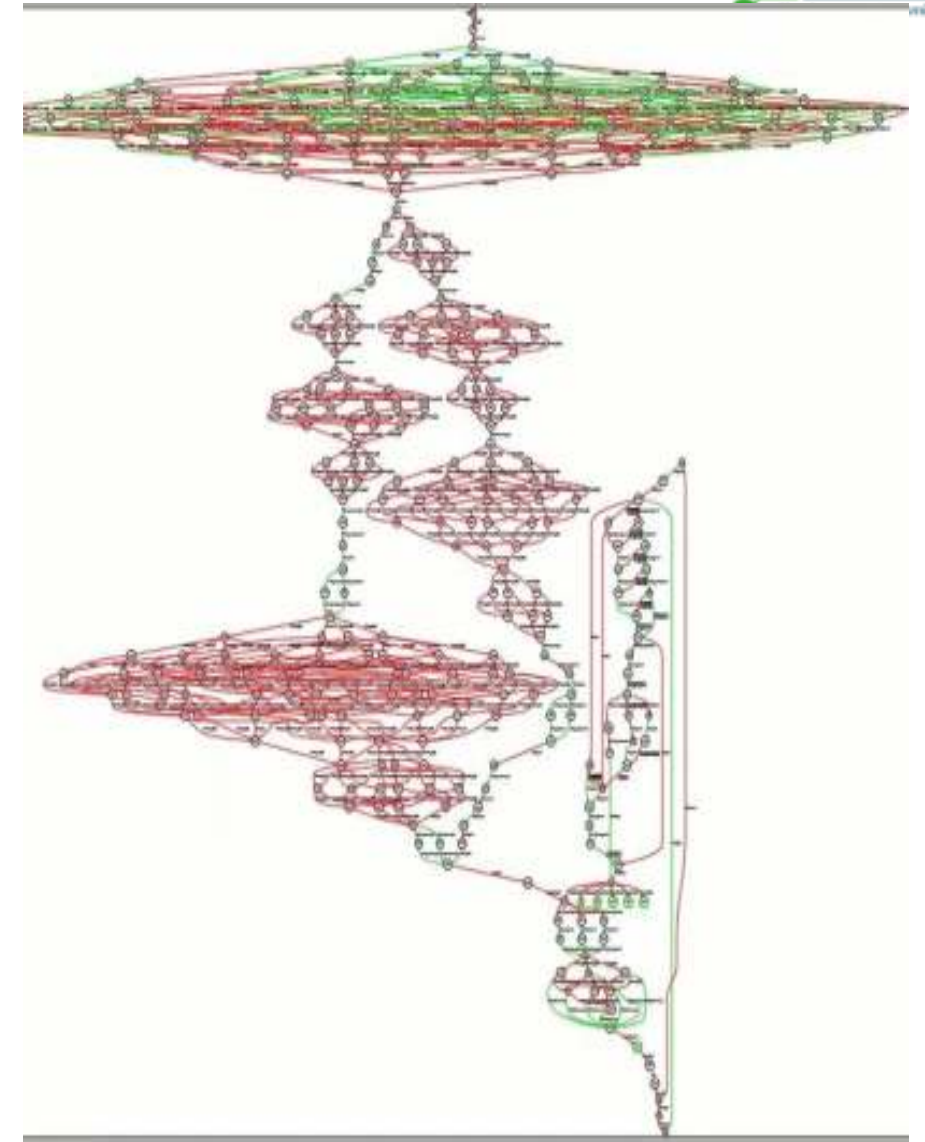
- Collaboration to understand the protection algorithm and its specs :
 - RWTH explanations about the different I/O
 - Simulink model given
- C code achievements :
 - Time based events translated into C functions (delays, ...)

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

IED PROTOTYPING

Supervisors: Implementation

- Board to IED :
 - Extraction to C functions (SUPREMICA)
 - Integrate to the IED
 - Structure I/O
 - Align to IED prototyping workflow



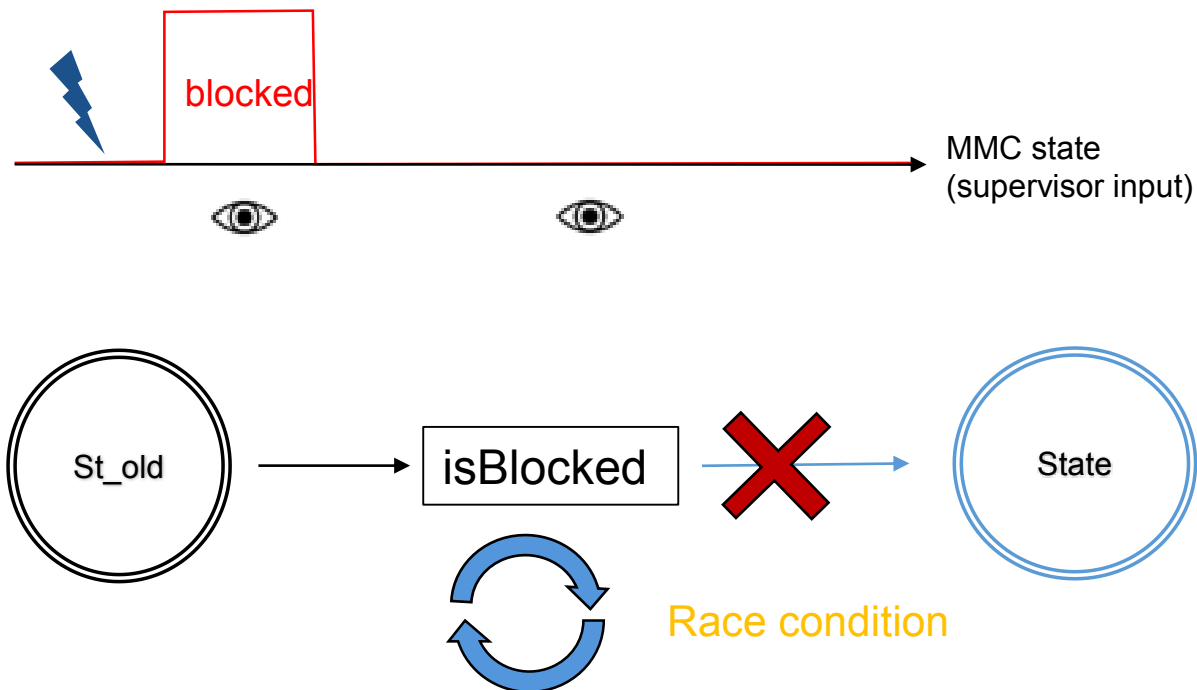
Supervisor State Diagram

SCOPE OF THE DEMONSTRATION - Hardware-in-the-loop setup

IED PROTOTYPING

Supervisors : Race condition

- Issue raised by HIL testing
- The supervisor is outside the simulation :
 - Not synchronized anymore



IED PROTOTYPING

Supervisors : Race condition fix

- Make the impulse long enough to make sure the supervisor see it.
 - Quick fix, but not robust
 - How do we choose the time ? What if there is a time delay non predictable ?



- Next step example : « Acknowledgement » :
 - Keep the pulse going and wait for an « Ok » answer from the supervisor.
 - Deeper research needed

SCOPE OF THE DEMONSTRATION

Application of the IEC61850 communication standard



Antoine
Ghyselinck



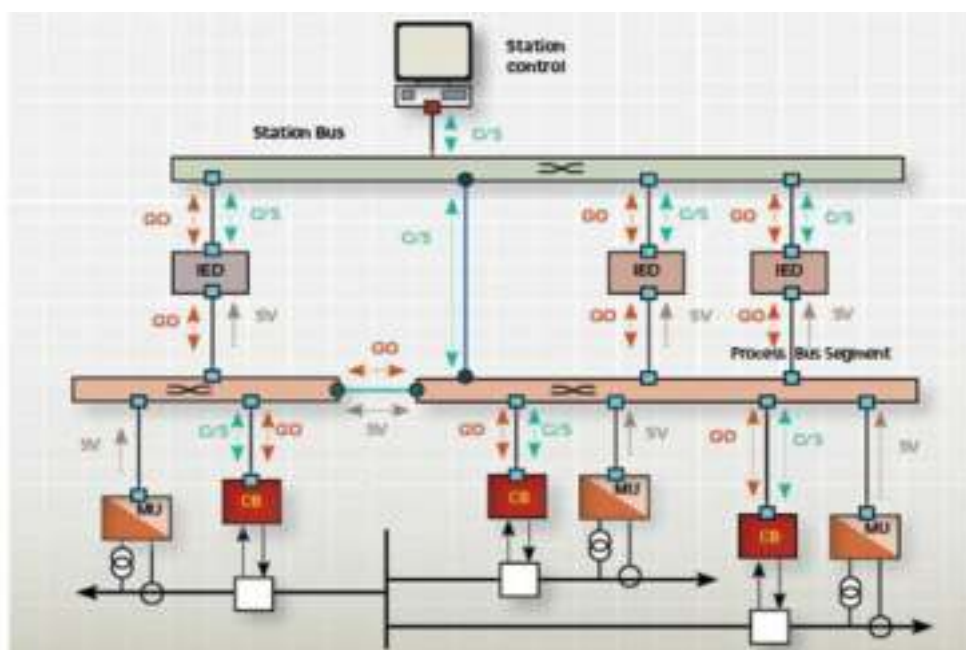
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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

SCOPE OF THE DEMONSTRATION - Application of the IEC61850 communication standard




IEC 61850



- Norm to transfer data between intelligent devices
- It was made for interoperability and rapidity. IEDs from different constructors can exchange data via IEC61850



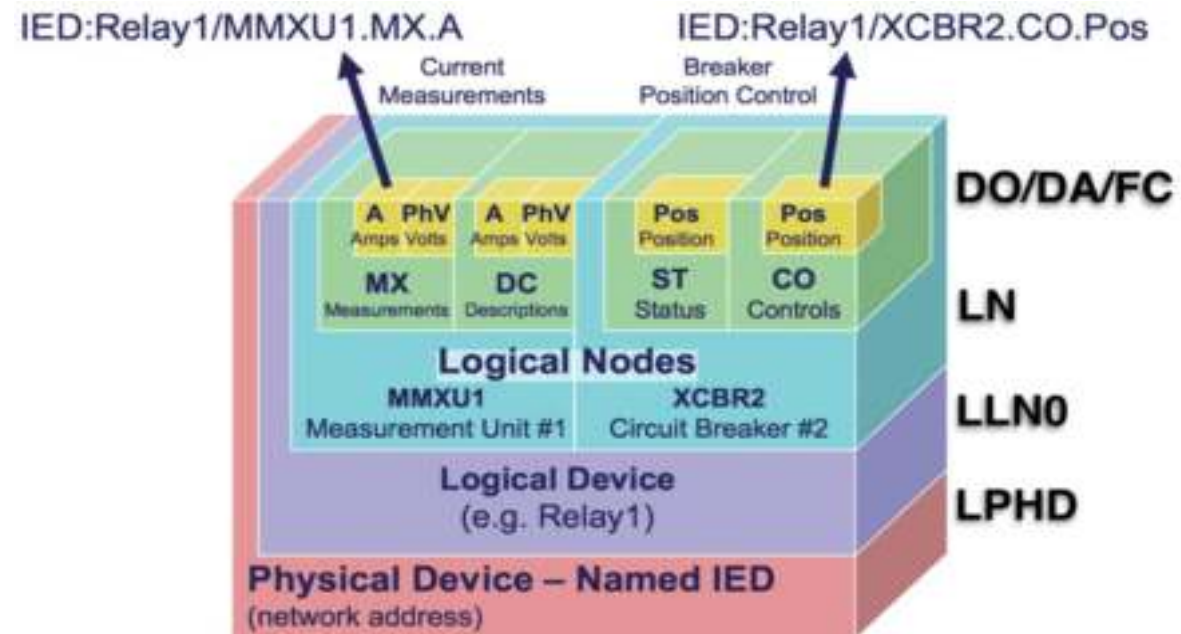
IEC61850 Example Architecture

Application layer	MMS	SV	GOOSE	SNTP
Presentation layer	Oriented Connection			
Session layer				
Transport layer				UDP TCP
Network layer	IP			IP
Data link layer	Ethernet			
Physical layer	Optical Fiber			

IEC61850 in the OSI model*

IEC61850: SEMANTICS

- Understanding semantics of the protocol
 - Object Oriented protocol
 - Messages :
 - Sampled Values (SV)
 - Generic Object Oriented Substation Event (GOOSE)



IEC61850: IMPLEMENTATION

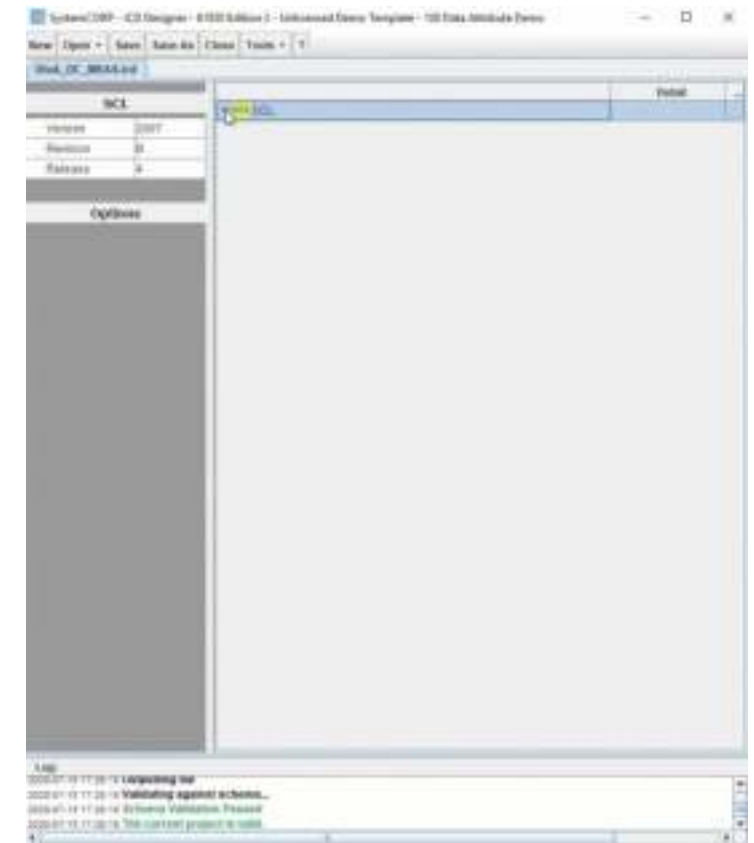
- Making HYPERSIM and RPI communicate with IEC61850

- IED capability description (ICD) files :
 - ICD Designer from SYSTEMCORP
 - Used in HYPERSIM to feed the IEC driver

- LibIEC61850 :

- Open source C library
- Used by the RPI

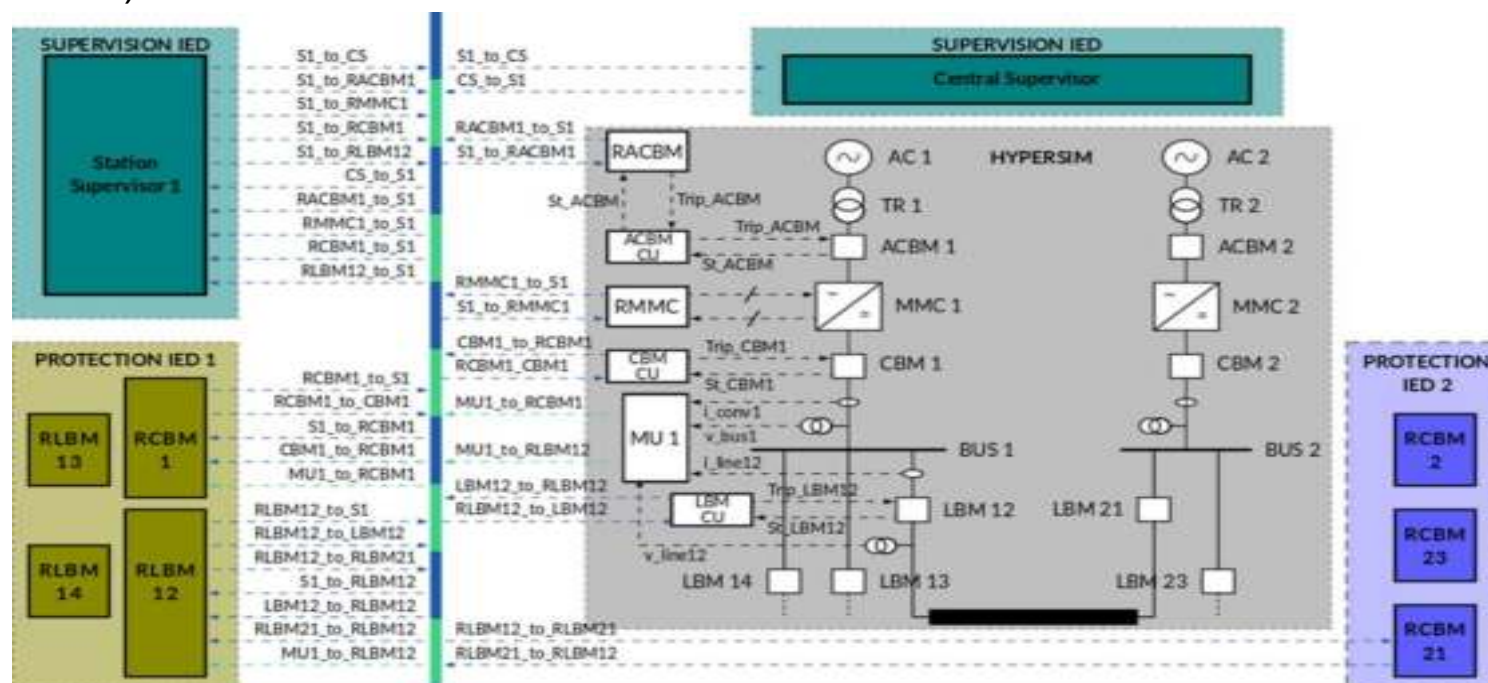
Data for one pole		
	CBS	FBS
Data points	234	104



ICD Designer

IEC61850: INTEGRATION

- Build the communication architecture :
 - Naming
 - Linking
 - Identification (MAC Address)



WIRESHARK : THE PACKET TRACER



Frame 140: 265 bytes on wire (2120 bits), 265 bytes captured (2120 bits) on interface 0

Ethernet II, Src: Raspberr_5e:df:2f (dc:a6:32:5e:df:2f), Dst: Iec-Tc57_01:10:a1 (01:0c:cd:01:10:a1)

GOOSE

APPID: 0x1000 (4096)

Length: 251

Reserved 1: 0x0000 (0)

Reserved 2: 0x0000 (0)

▼ goosPdu

gocbRef: StationSupervisorRMMC_Interface/LLN0\$G0\$CG_SS_P_1 to RMMC_P_1

timeAllowedtoLive: 0

datSet: StationSupervisorRMMC_Interface/LLN0\$G0\$CG_SS_P_1 to RMMC_P_1

goID: StationSupervisorRMMC_Interface/LLN0\$G0\$CG_SS_P_1 to RMMC_P_1

t: Jul 21, 2020 12:51:39.88799951 UTC

stNum: 7

sqNum: 0

test: False

confRev: 1

ndsCom: False

numDatSetEntries: 6

▼ allData: 6 items

- ▼ Data: integer (5)
 - integer: 2
- ▼ Data: integer (5)
 - integer: 1
- ▼ Data: integer (5)
 - integer: 1
- ▼ Data: integer (5)
 - integer: 3
- ▼ Data: integer (5)
 - integer: 0
- ▼ Data: integer (5)
 - integer: 1

0000 01 0c cd 01 10 a1 dc a6 32 5e df 2f 88 b0 10 00 2"/...

0010 00 fb 00 00 00 00 01 81 10 80 3d 53 74 61 74 09a---Stat1

0020 6f 6e 53 75 70 65 72 76 69 73 6f 72 52 4d 4d 43 onSuperv isorRMMC

0030 5f 49 6e 74 65 72 66 61 63 65 2f 4c 4e 30 24 Interfa ce/LLN0\$

0040 47 4f 24 43 47 5f 53 53 5f 50 5f 31 5f 74 6f 5f GO\$CG SS_P_1 to

0050 52 4d 4d 43 5f 50 5f 31 81 01 00 02 3d 53 74 61 RMMC_P_1 ----Sta

0060 74 69 6f 6e 53 75 70 65 72 76 69 73 6f 72 52 4d tionSuperv isorRM

0070 4d 43 5f 49 6e 74 65 72 66 61 63 65 2f 4c 4e 4e MC Inter face/LLN

0080 30 24 47 4f 24 43 47 5f 53 53 5f 50 5f 31 5f 74 0\$G0\$CG SS_P_1 t

0090 6f 5f 52 4d 4d 43 5f 50 5f 31 83 3d 53 74 61 74 o RMMC_P_1 ->Stat

00a0 69 6f 6e 53 75 70 65 72 76 69 73 6f 72 52 4d 4d ionSuper visorRMM

00b0 43 5f 49 6e 74 65 72 66 61 63 65 2f 4c 4e 30 C Interf ace/LLN0

00c0 24 47 4f 24 43 47 5f 53 5f 50 5f 31 5f 74 6f \$G0\$CG S S_P_1 to

00d0 5f 52 4d 4d 43 5f 50 5f 31 84 00 5f 16 e4 db a3 RMMC_P_1 ----

00e0 53 7f 0a 05 01 07 06 01 00 87 01 00 00 01 01 09 \$-----

00f0 01 00 0a 01 06 ab 12 05 01 02 05 01 01 05 01 07 -----

0100 05 01 03 05 01 00 05 01 01 -----

GOOSE Message

Identification

Naming Linking

Content

RESULTS OF THE HARDWARE-IN-THE-LOOP DEMONSTRATION



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Garcia



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VIRTUAL DEMO CONVERTER BREAKER PROTECTION STRATEGY

Startup



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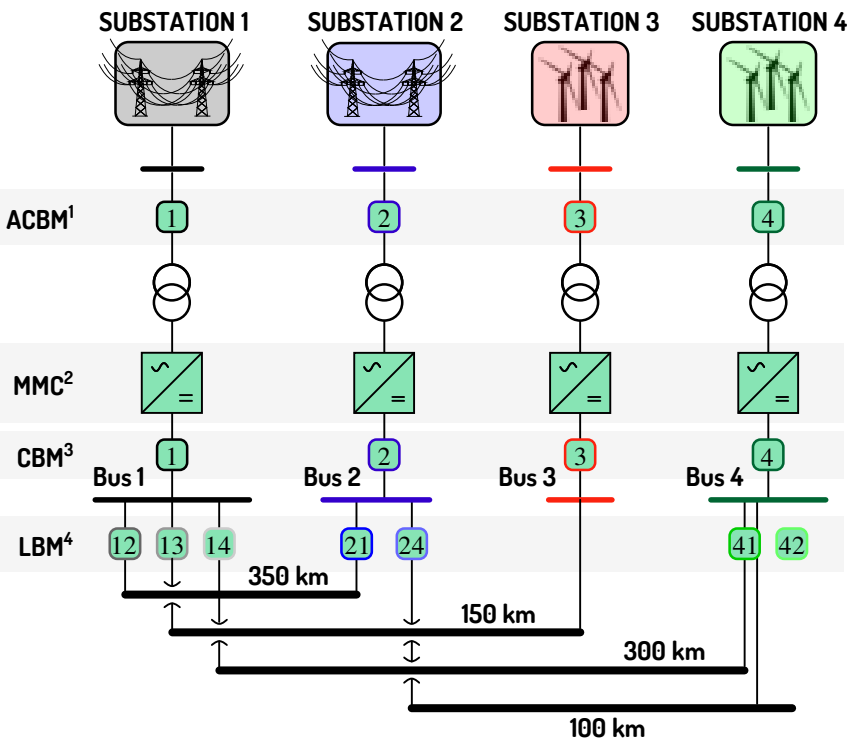
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RESULTS OF THE HIL DEMONSTRATION

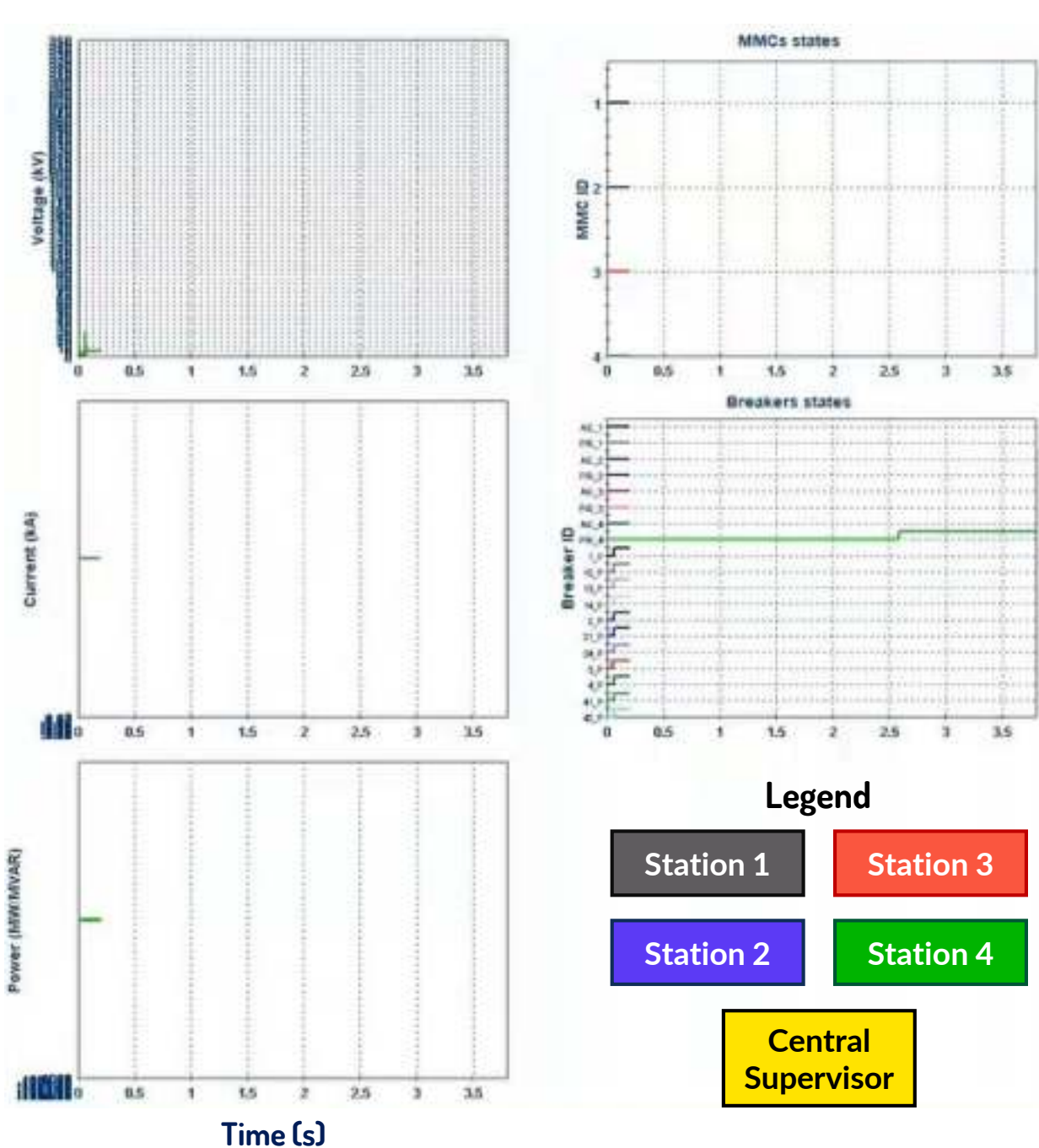
FOUR-TERMINAL HVDC NETWORK

Half-bridge MMC converters

Startup



¹ AC breaker module
² Modular multi-level converter
³ Converter breaker module
⁴ Line breaker module

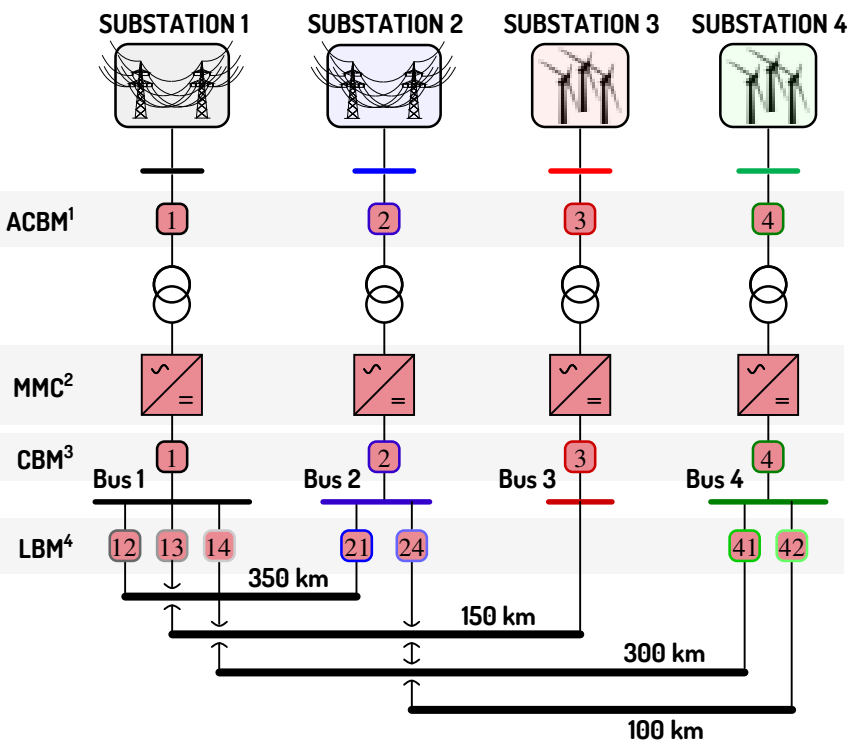


RESULTS OF THE HIL DEMONSTRATION

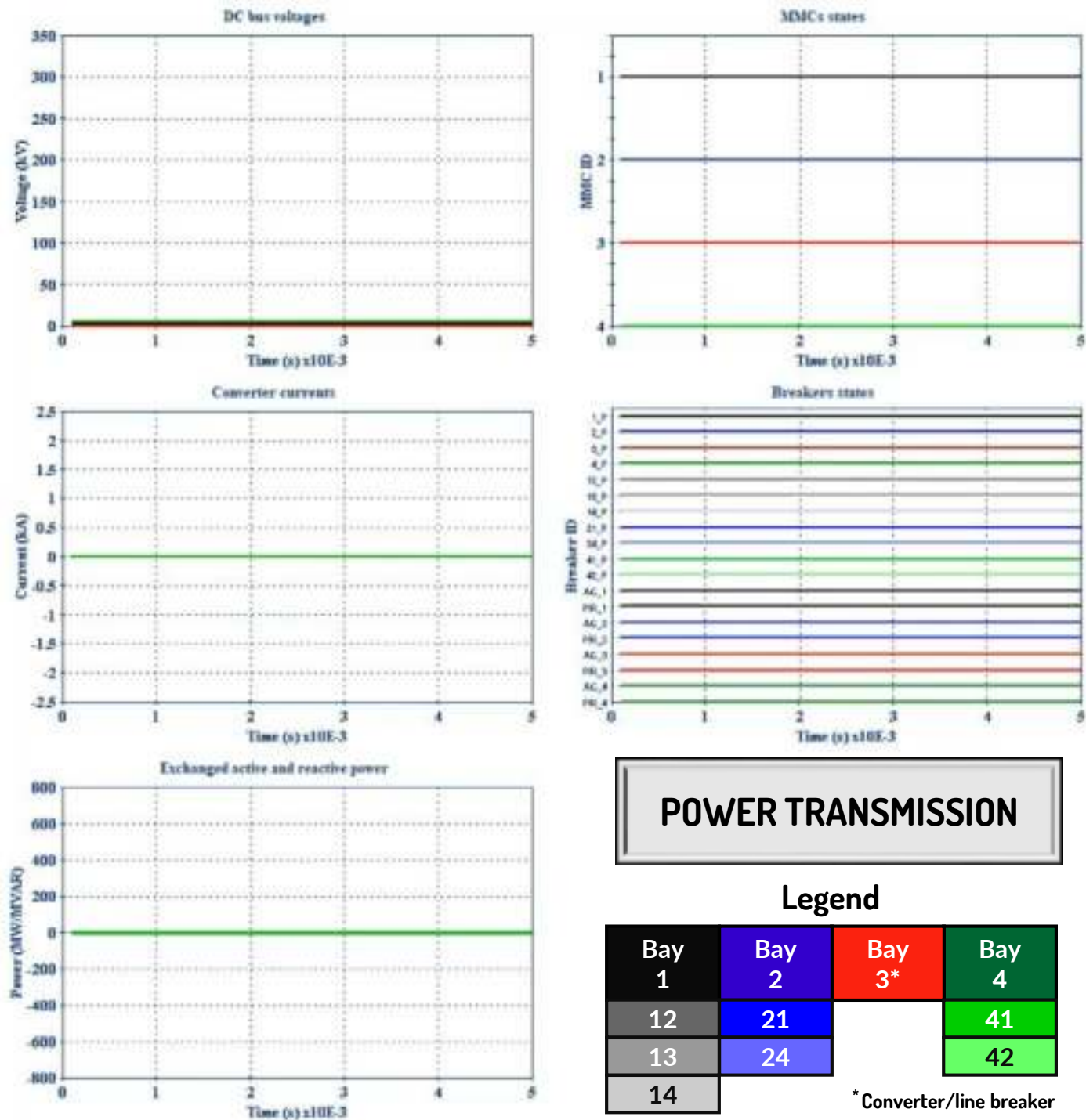
FOUR-TERMINAL HVDC NETWORK

Half-bridge MMC converters

Startup



- ¹ AC breaker module
- ² Modular multi-level converter
- ³ Converter breaker module
- ⁴ Line breaker module



VIRTUAL DEMO CONVERTER BREAKER PROTECTION STRATEGY

Pole-to-ground fault in cable 24



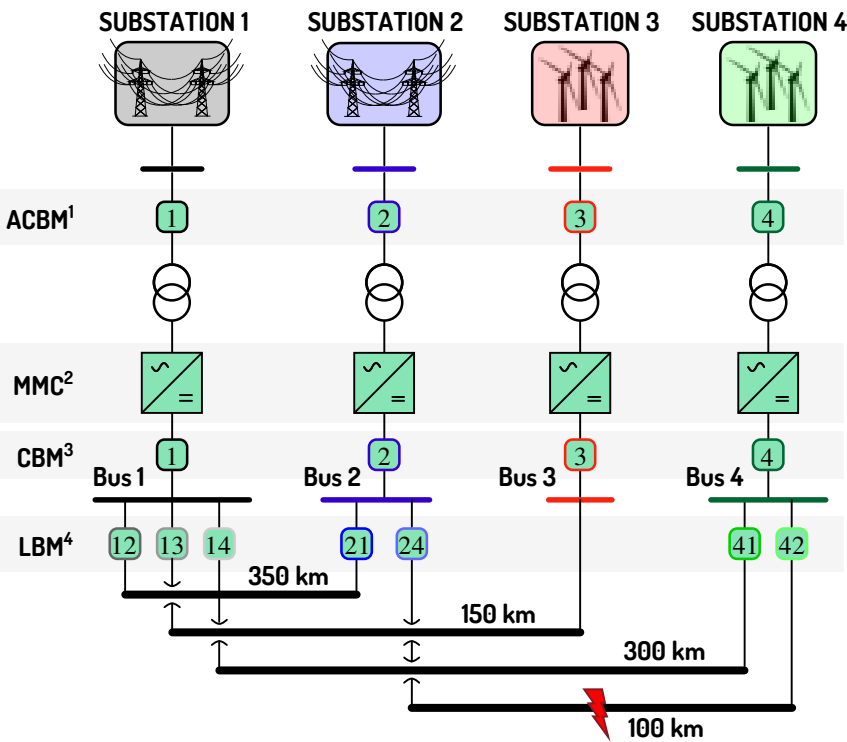
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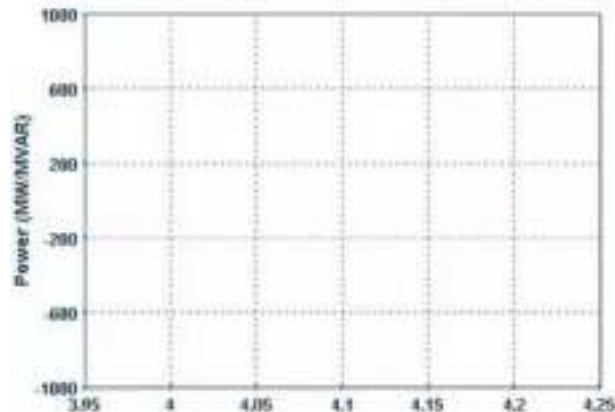
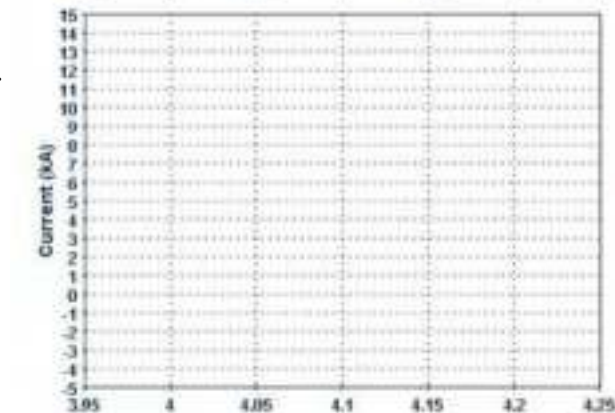
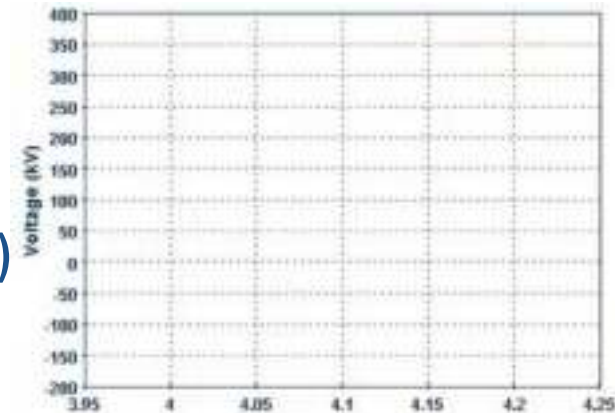
RESULTS OF THE HIL DEMONSTRATION

CONVERTER BREAKER PROTECTION STRATEGY

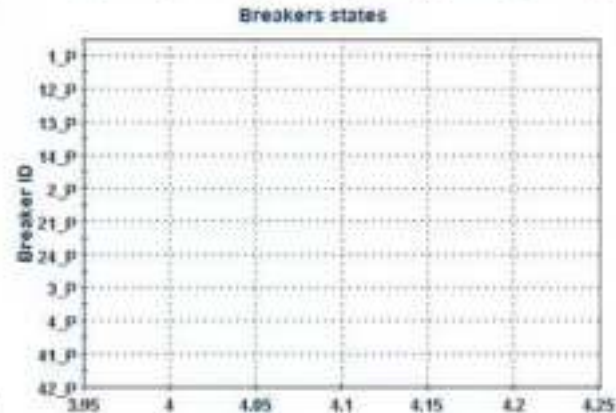
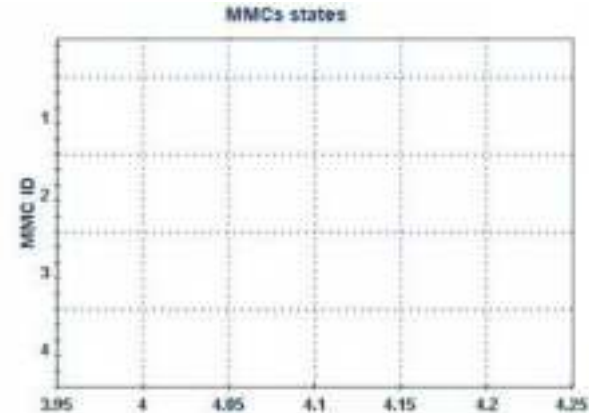
Pole-to-ground fault: cable 24 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Converter breaker module
⁴ Line breaker module



Time (s)



Legend

Station 1

Station 3

Station 2

Station 4

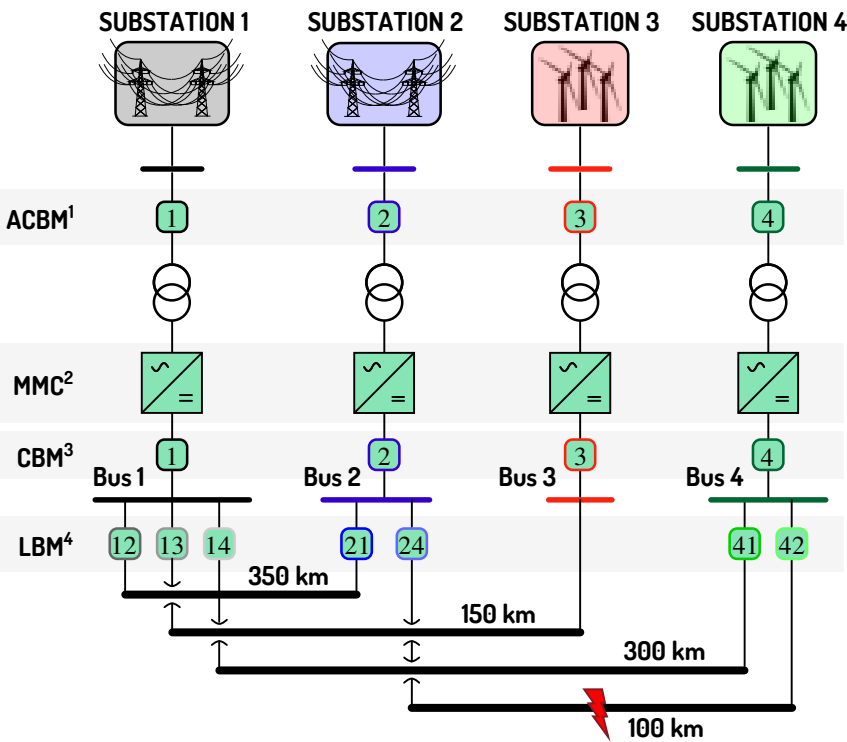
Central Supervisor

Time	Source	Protocol
0.0000000	Raspberr 73:92:64	GOOSE
0.000017185	Raspberr 59:0a:20	GOOSE
0.000547302	Raspberr 73:92:64	GOOSE
0.000553226	Raspberr 59:0a:20	GOOSE
0.001272026	Raspberr 59:0a:11	GOOSE
0.001582612	Raspberr 5e:de:4c	GOOSE
0.002123007	Raspberr 5e:de:4c	GOOSE
0.002691939	Raspberr 73:92:6d	GOOSE
0.002736808	Raspberr 73:92:07	GOOSE
0.003266777	Raspberr 73:92:07	GOOSE
0.003573530	Raspberr 5e:df:2f	GOOSE
0.004481157	Raspberr 73:92:61	GOOSE
0.006585665	Raspberr 59:0a:23	GOOSE
0.006614627	Raspberr 59:0a:23	GOOSE
0.006636497	Raspberr 59:0a:23	GOOSE
0.006655478	Raspberr 59:0a:23	GOOSE
0.007718547	Raspberr 73:92:61	GOOSE
0.007783305	Raspberr 59:0a:11	GOOSE
0.007870062	Raspberr 5e:df:2f	GOOSE
0.008020018	Raspberr 73:92:6d	GOOSE
0.008546285	Raspberr 58:e8:19	GOOSE
0.008893094	Raspberr 73:92:76	GOOSE
0.008961445	Raspberr 73:92:52	GOOSE
0.009000000	Raspberr 73:92:52	GOOSE
0.009527635	Raspberr 73:92:52	GOOSE
0.009602356	Raspberr 73:92:64	GOOSE
0.009607597	Raspberr 59:0a:20	GOOSE
0.009741223	Raspberr 58:e8:19	GOOSE
0.010079049	Raspberr 59:0a:11	GOOSE
0.010088826	Raspberr 5e:df:2f	GOOSE
0.010093197	Raspberr 73:92:52	GOOSE
0.010299988	Raspberr 58:e8:19	GOOSE
0.010881642	Raspberr 73:92:58	GOOSE
0.011033824	Raspberr 73:92:61	GOOSE
0.011077304	Raspberr 58:e7:43	GOOSE
0.011139432	Raspberr 5e:de:4c	GOOSE
0.011212356	Raspberr 73:92:6d	GOOSE
0.011258170	Raspberr 73:92:6d	GOOSE
0.011265948	Raspberr 59:0a:11	GOOSE
0.011479962	Raspberr 73:92:19	GOOSE
0.011991154	Raspberr 73:92:07	GOOSE
0.013092406	Raspberr 73:92:07	GOOSE
0.013110295	Raspberr 73:92:07	GOOSE
0.013523508	Raspberr 5e:df:2f	GOOSE
0.014398451	Raspberr 73:92:6d	GOOSE
0.014585206	Raspberr 5e:df:2f	GOOSE
0.014700725	Raspberr 73:92:58	GOOSE
0.015091454	Raspberr 73:92:76	GOOSE
0.015211541	Raspberr 59:0a:11	GOOSE
0.015497611	Raspberr 73:92:6d	GOOSE
0.015715736	Raspberr 5e:df:2f	GOOSE
0.016326180	Raspberr 73:92:6d	GOOSE
0.019737570	Raspberr 73:92:52	GOOSE
0.019899419	Raspberr 58:e8:19	GOOSE
0.031272031	Raspberr 59:0a:20	GOOSE
0.031672892	Raspberr 73:92:64	GOOSE
0.032981213	Raspberr 5e:de:4c	GOOSE
0.034229686	Raspberr 73:92:07	GOOSE
0.050417782	Raspberr 59:0a:23	GOOSE
0.050460670	Raspberr 59:0a:23	GOOSE

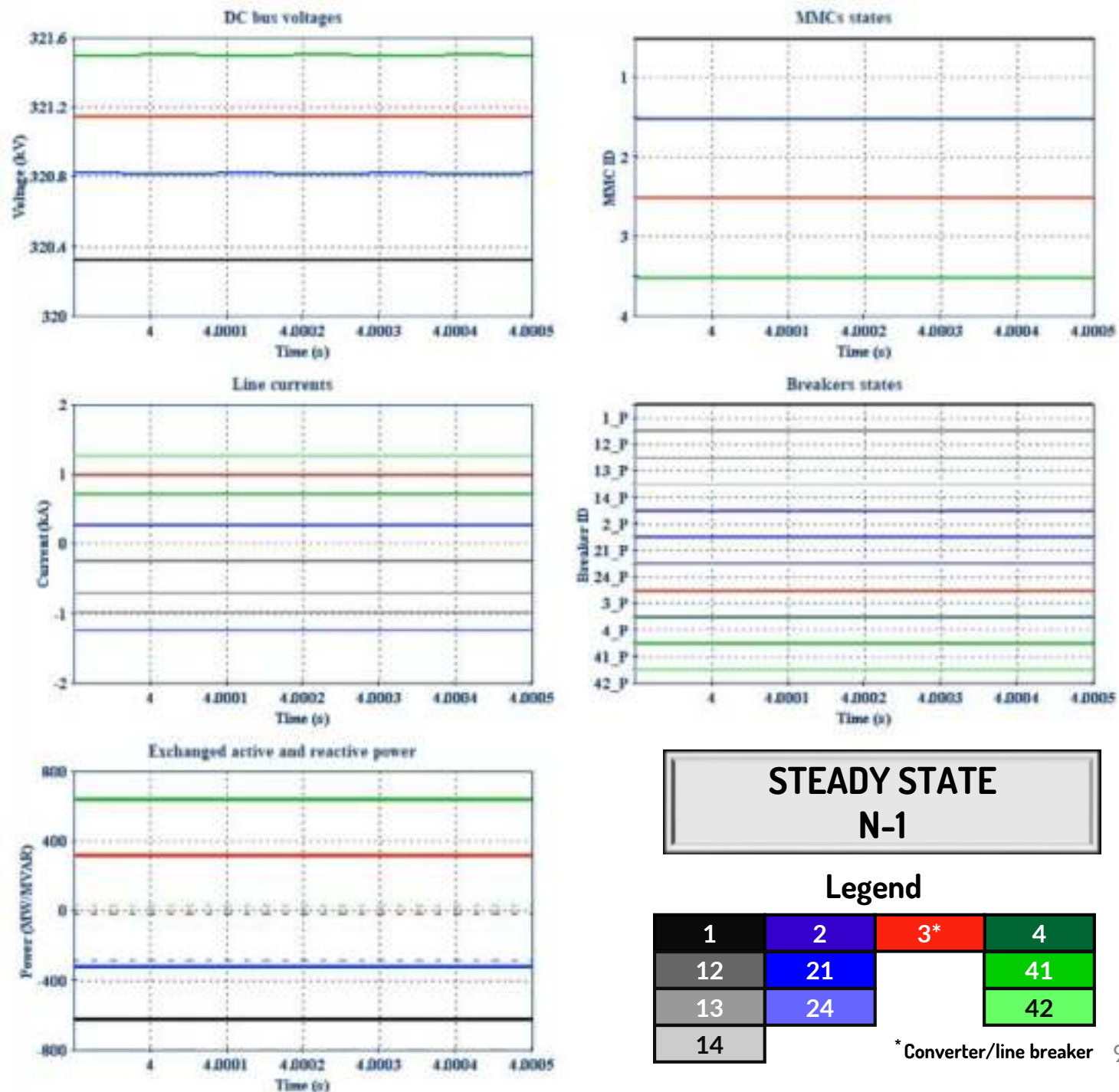
RESULTS OF THE HIL DEMONSTRATION

CONVERTER BREAKER PROTECTION STRATEGY

Pole-to-ground fault: cable 24 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Converter breaker module
⁴ Line breaker module



STEADY STATE
N-1

Legend

1	2	3*	4
12	21		41
13	24		42
14			

* Converter/line breaker

VIRTUAL DEMO CONVERTER BREAKER PROTECTION STRATEGY

Pole-to-ground fault in cable 13
Backup sequence: CBM1 fails to open

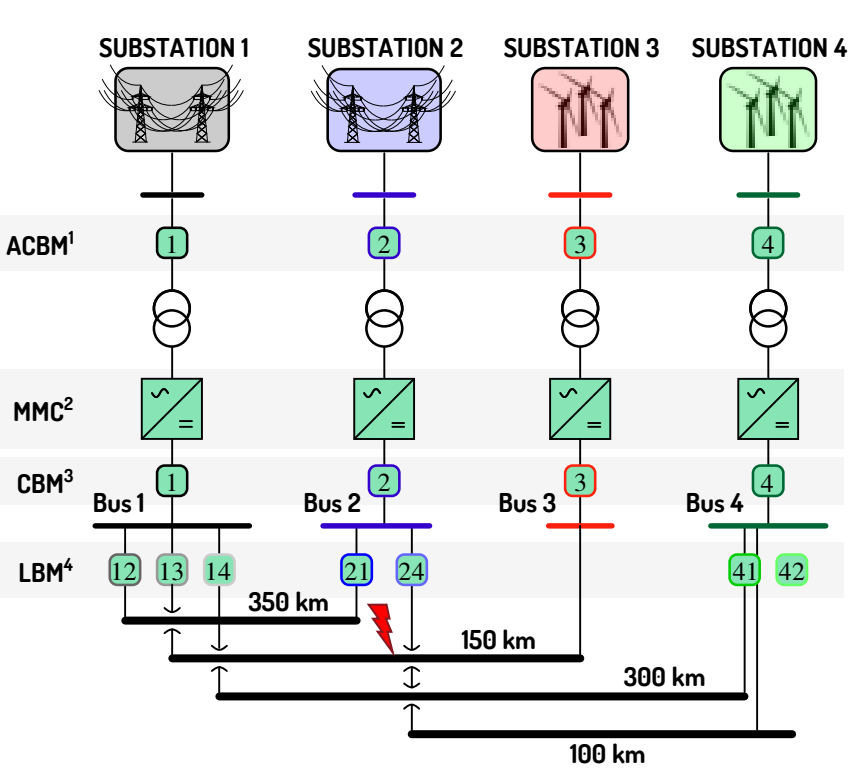


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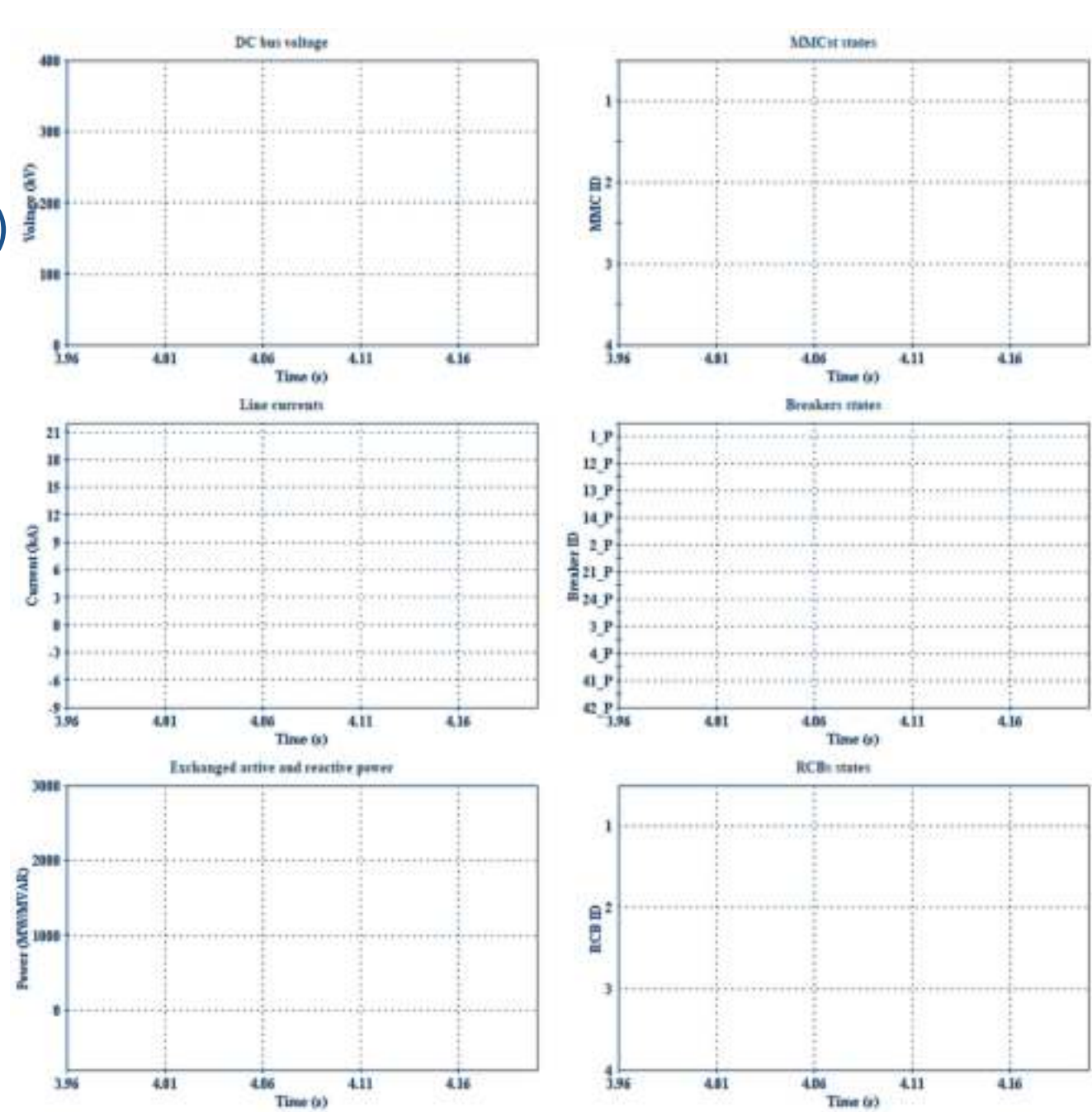
RESULTS OF THE HIL DEMONSTRATION

CONVERTER BREAKER PROTECTION STRATEGY

Pole-to-ground fault: cable 13 (@75km)
Backup sequence: CBM1 fails to open



¹ AC breaker module
² Modular multi-level converter
³ Converter breaker module
⁴ Line breaker module

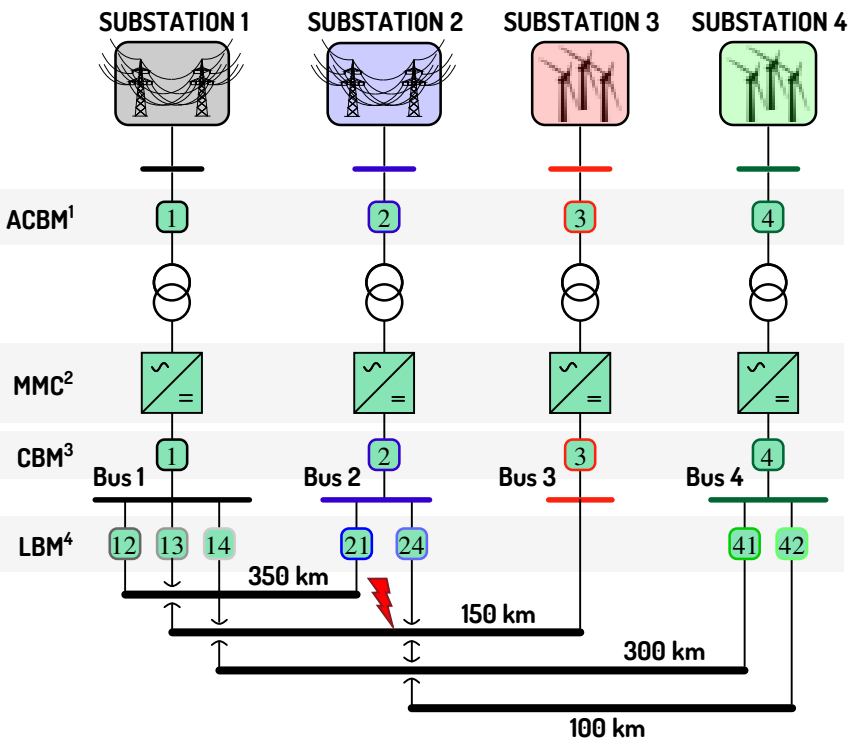


Time	Source	Protocol
0.00000000	Raspberr 73:92:07:0005E	
0.000333881	Raspberr 5e:de:4c:0005E	
0.000357095	Raspberr 73:92:07:0005E	
0.000503551	Raspberr 5e:de:4c:0005E	
0.001334211	Raspberr 73:92:07:0005E	
0.002004516	Raspberr 59:0a:20:0005E	
0.002745143	Raspberr 73:92:07:0005E	
0.003070617	Raspberr 5e:df:2f:0005E	
0.003130056	Raspberr 59:0a:20:0005E	
0.003766090	Raspberr 73:92:07:0005E	
0.004791319	Raspberr 59:0a:11:0005E	
0.006637519	Raspberr 73:92:07:0005E	
0.008791064	Raspberr 73:92:19:0005E	
0.009061021	Raspberr 73:92:07:0005E	
0.009313064	Raspberr 73:92:19:0005E	
0.009540062	Raspberr 58:e7:43:0005E	
0.009840053	Raspberr 73:92:19:0005E	
0.010700027	Raspberr 73:92:07:0005E	
0.010315473	Raspberr 73:92:07:0005E	
0.010414504	Raspberr 73:92:19:0005E	
0.011267139	Raspberr 73:92:07:0005E	
0.011311715	Raspberr 73:92:19:0005E	
0.011573073	Raspberr 5e:df:2f:0005E	
0.011900660	Raspberr 73:92:07:0005E	
0.012210933	Raspberr 59:0a:20:0005E	
0.013450498	Raspberr 73:92:07:0005E	
0.016333712	Raspberr 58:e7:43:0005E	
0.016338360	Raspberr 73:92:19:0005E	
0.019373885	Raspberr 59:0a:23:0005E	
0.019403736	Raspberr 59:0a:23:0005E	
0.019430310	Raspberr 59:0a:23:0005E	
0.019453383	Raspberr 59:0a:23:0005E	
0.019511151	Raspberr 73:92:19:0005E	
0.019811460	Raspberr 58:e7:43:0005E	
0.020102013	Raspberr 5e:df:2f:0005E	
0.020211440	Raspberr 73:92:19:0005E	
0.020307677	Raspberr 59:0a:11:0005E	
0.020513749	Raspberr 73:92:07:0005E	
0.022230951	Raspberr 5e:df:2f:0005E	
0.023102000	Raspberr 58:e7:43:0005E	
0.023503960	Raspberr 73:92:19:0005E	
0.023719280	Raspberr 59:0a:11:0005E	
0.023944488	Raspberr 73:92:07:0005E	
0.025123591	Raspberr 73:92:07:0005E	
0.027101000	Raspberr 73:92:07:0005E	
0.031995142	Raspberr 5e:de:4c:0005E	
0.034100260	Raspberr 73:92:07:0005E	
0.034209010	Raspberr 59:0a:20:0005E	
0.035302302	Raspberr 5e:de:4c:0005E	
0.037270303	Raspberr 5e:df:2f:0005E	
0.038271404	Raspberr 73:92:07:0005E	
0.038335575	Raspberr 5e:df:2f:0005E	
0.039451662	Raspberr 5e:df:2f:0005E	
0.041592614	Raspberr 5e:df:2f:0005E	
0.041860590	Raspberr 73:92:07:0005E	
0.043157076	Raspberr 73:92:07:0005E	
0.043960321	Raspberr 73:92:07:0005E	
0.072000014	Raspberr 59:0a:23:0005E	
0.072822000	Raspberr 59:0a:23:0005E	
0.072839421	Raspberr 59:0a:23:0005E	
0.072063272	Raspberr 59:0a:23:0005E	
0.073170099	Raspberr 73:92:07:0005E	
0.073961711	Raspberr 5e:df:2f:0005E	

RESULTS OF THE HIL DEMONSTRATION

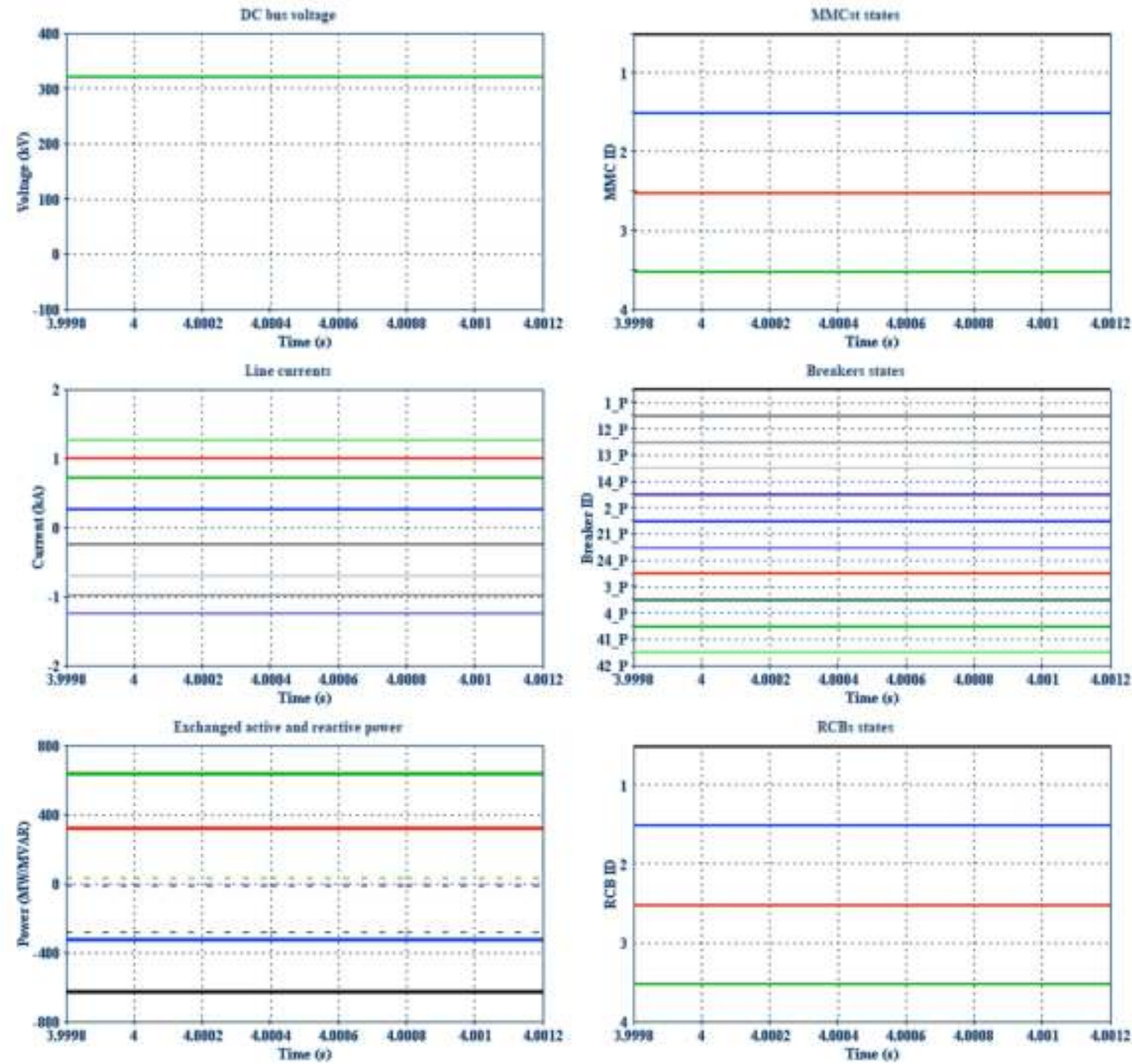
CONVERTER BREAKER PROTECTION STRATEGY

Pole-to-ground fault: cable 13 (@75km)
Backup sequence: CBM1 fails to open



¹ AC breaker module
² Modular multi-level converter
³ Converter breaker module
⁴ Line breaker module

STEADY STATE
N-1



VIRTUAL DEMO FULL-BRIDGE CONVERTER PROTECTION STRATEGY

Pole-to-ground fault in cable 13

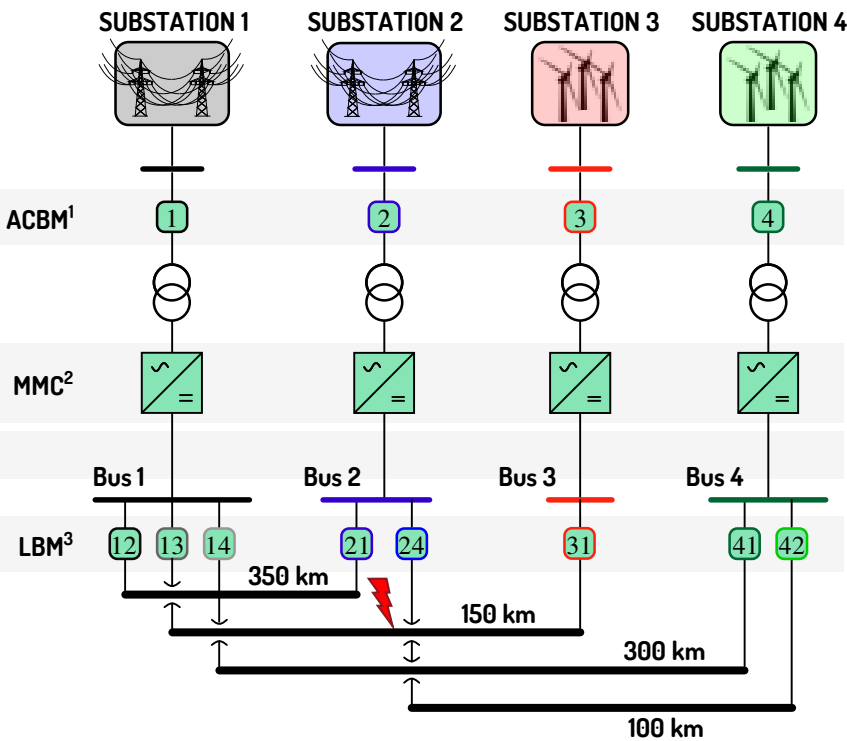


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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 691714.

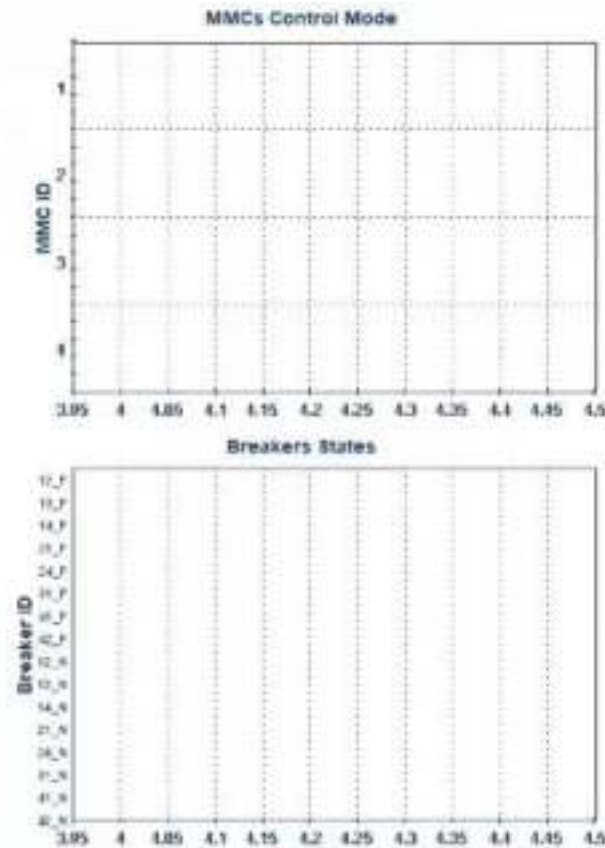
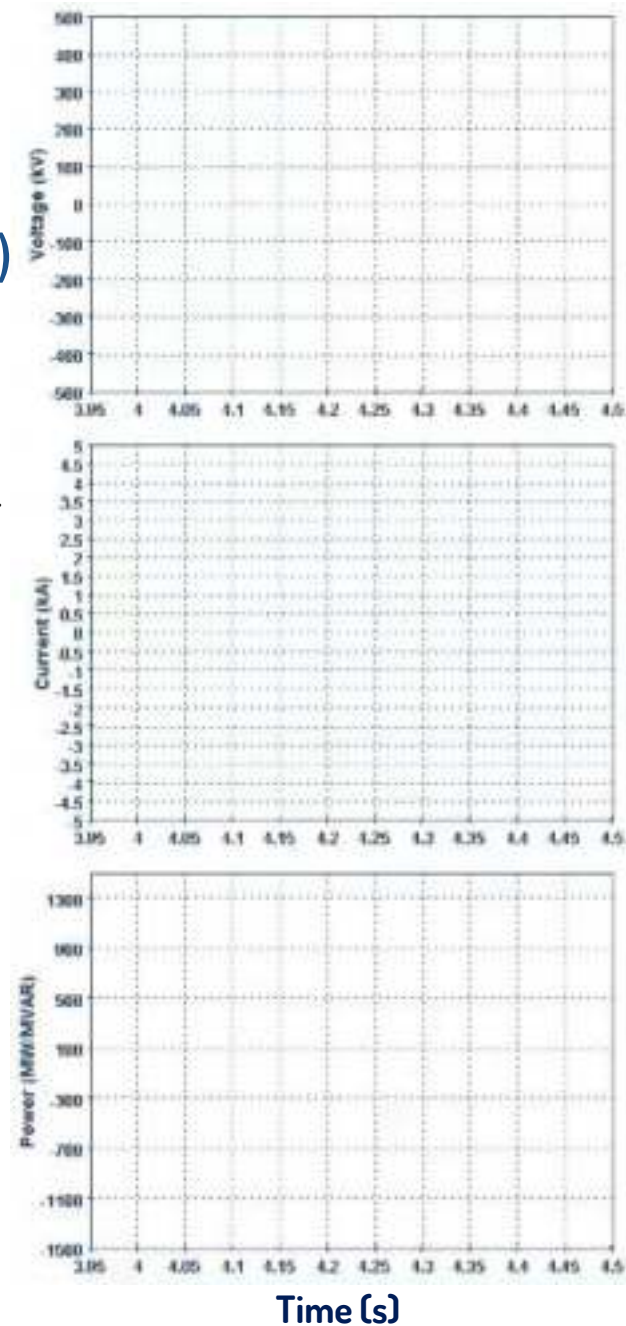
RESULTS OF THE HIL DEMONSTRATION

FULL-BRIDGE CONVERTER-BASED PROTECTION STRATEGY

Pole-to-ground fault: cable 13 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Line breaker module



Time	Source	Protocol
0.00000000	Raspberr 73:92:58	GOOSE
0.000094238	Raspberr 73:92:07	GOOSE
0.000220532	Raspberr 58:e7:43	GOOSE
0.000231046	Raspberr 73:92:19	GOOSE
0.001009045	Raspberr 73:91:1b	GOOSE
0.001335673	Raspberr 73:92:52	GOOSE
0.001632333	Raspberr 73:92:76	GOOSE
0.001778626	Raspberr 58:e8:19	GOOSE
0.010509463	Raspberr 73:92:76	GOOSE
0.010678006	Raspberr 73:91:1b	GOOSE
0.010696980	Raspberr 73:92:07	GOOSE
0.010817032	Raspberr 58:e8:19	GOOSE
0.010932993	Raspberr 58:e7:43	GOOSE
0.011667106	Raspberr 73:92:19	GOOSE
0.012063060	Raspberr 73:92:52	GOOSE
0.014131865	Raspberr 73:92:58	GOOSE
0.014203937	Raspberr 73:92:58	GOOSE
0.015043937	Raspberr 73:92:07	GOOSE
0.050905716	Raspberr 73:92:58	GOOSE
0.051322188	Raspberr 73:92:07	GOOSE
0.051919100	Raspberr 73:92:07	GOOSE
0.052534735	Raspberr 73:92:07	GOOSE
0.063897903	Raspberr 73:92:58	GOOSE
0.065013507	Raspberr 73:92:58	GOOSE
0.066150611	Raspberr 73:92:58	GOOSE
0.166230583	Raspberr 73:92:58	GOOSE

Station 1

Station 2

Station 3

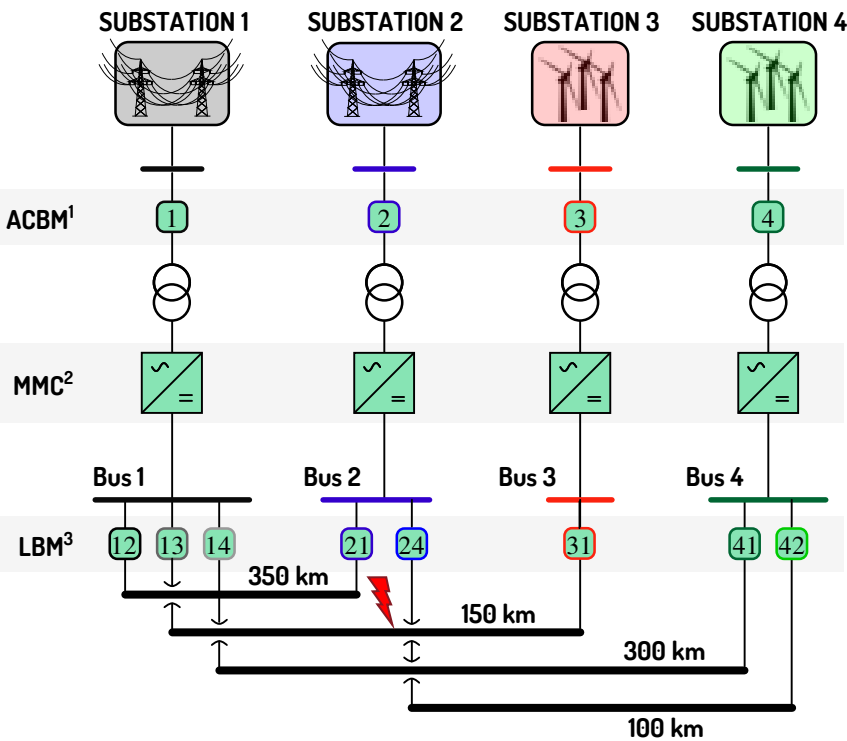
Station 4

Central Supervisor

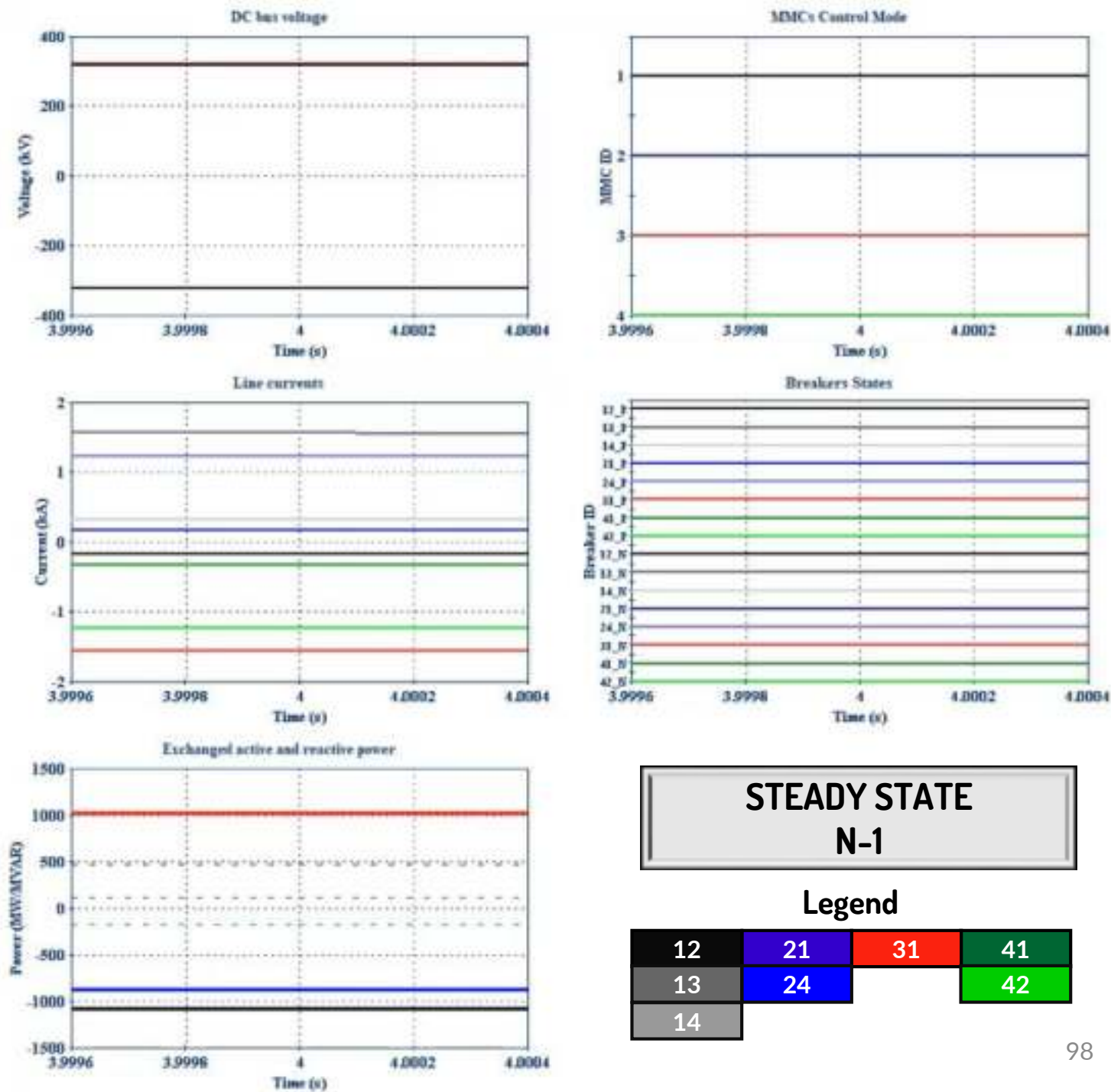
RESULTS OF THE HIL DEMONSTRATION

FULL-BRIDGE CONVERTER-BASED PROTECTION STRATEGY

Pole-to-ground fault: cable 13 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Line breaker module



VIRTUAL DEMO FULL-BRIDGE CONVERTER PROTECTION STRATEGY

Pole-to-pole fault in cable 24

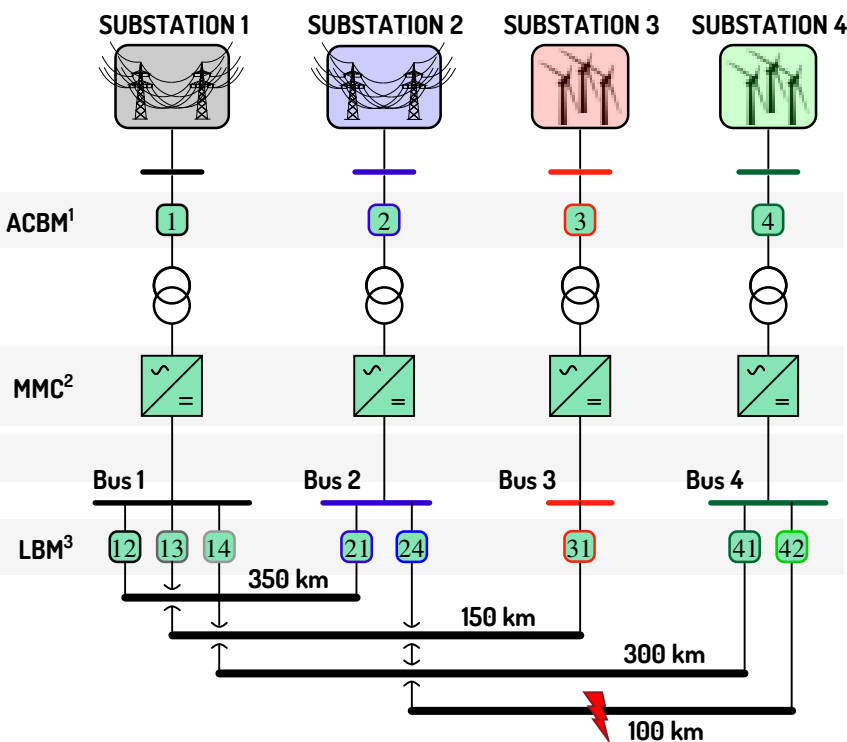


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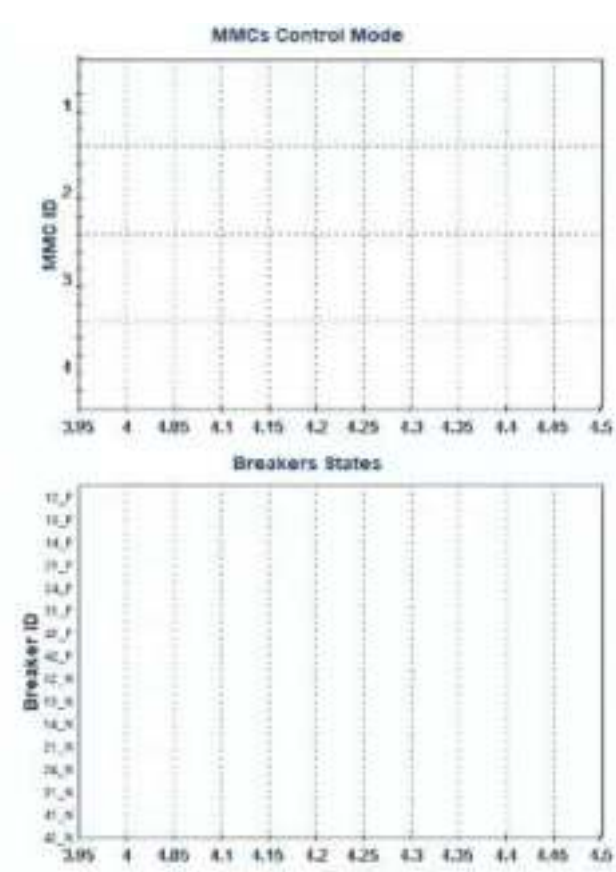
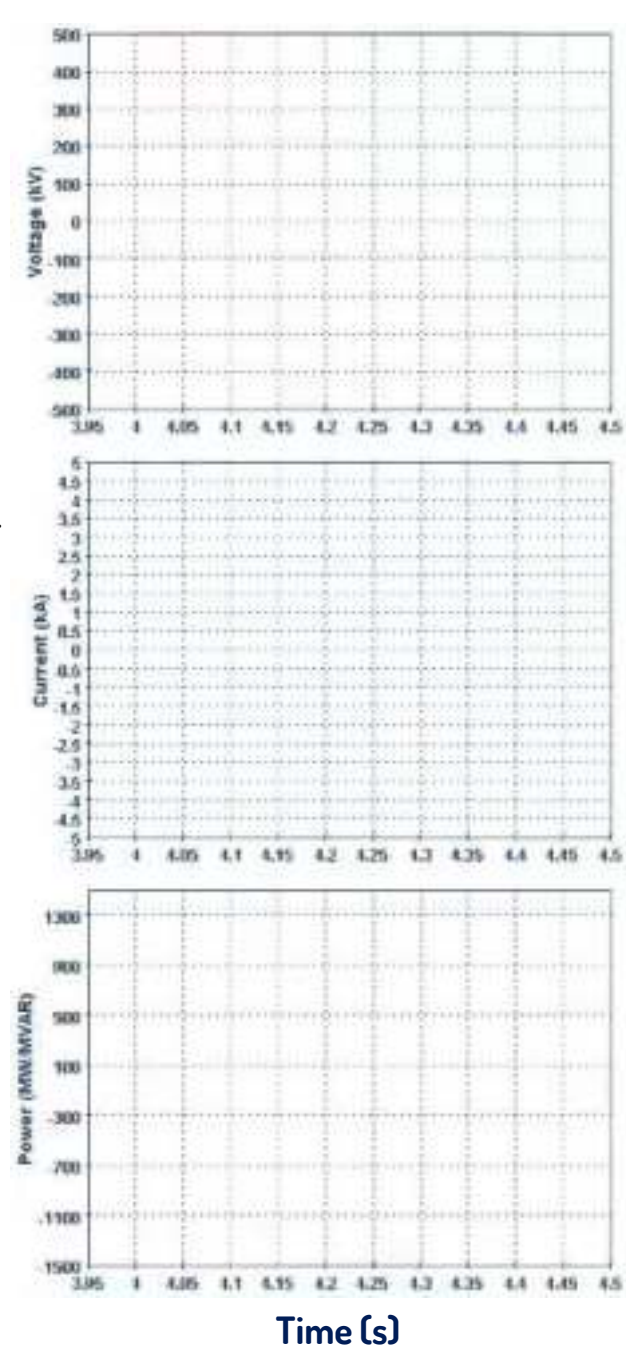
RESULTS OF THE HIL DEMONSTRATION

FULL-BRIDGE CONVERTER-BASED PROTECTION STRATEGY

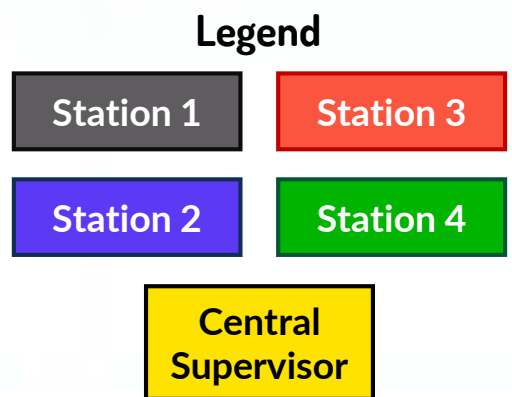
Pole-to-pole fault: cable 24 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Line breaker module



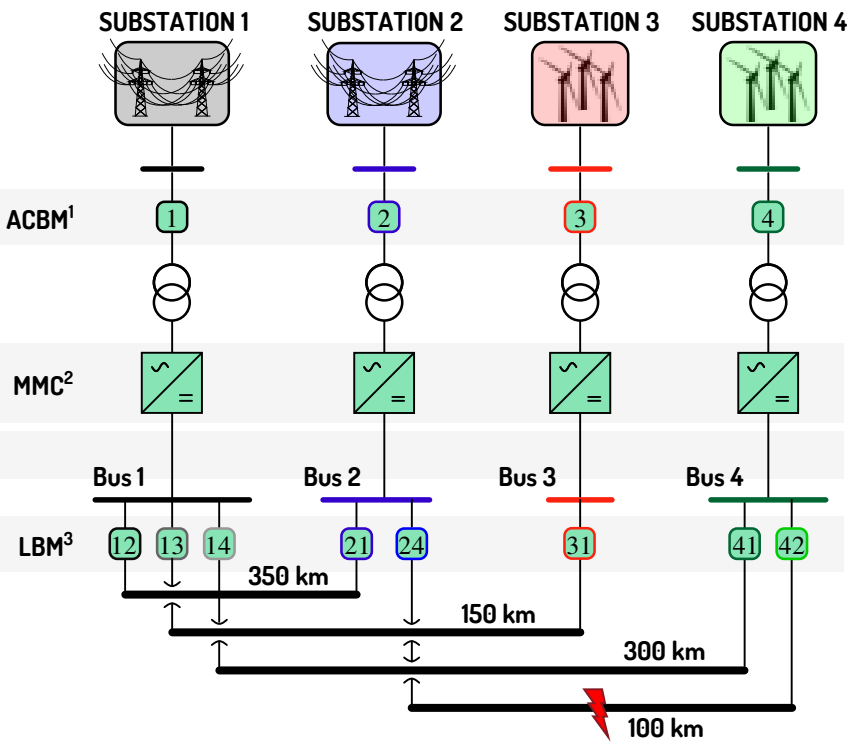
Time	Source	Protocol
0.00000000	Raspberr 58:e8:19	GOOSE
0.000220680	Raspberr 73:92:76	GOOSE
0.000418638	Raspberr 73:91:fb	GOOSE
0.000433508	Raspberr 73:92:52	GOOSE
0.001271415	Raspberr 73:92:58	GOOSE
0.001286155	Raspberr 73:92:19	GOOSE
0.001375301	Raspberr 58:e7:43	GOOSE
0.002125358	Raspberr 73:92:07	GOOSE
0.010229246	Raspberr 73:92:19	GOOSE
0.011435107	Raspberr 73:92:76	GOOSE
0.011644602	Raspberr 58:e8:19	GOOSE
0.011745766	Raspberr 58:e7:43	GOOSE
0.011807117	Raspberr 73:92:07	GOOSE
0.011885226	Raspberr 73:91:fb	GOOSE
0.014506203	Raspberr 73:92:52	GOOSE
0.014571461	Raspberr 73:92:52	GOOSE
0.014985192	Raspberr 58:e8:19	GOOSE
0.015061190	Raspberr 73:92:52	GOOSE
0.015397608	Raspberr 73:92:58	GOOSE
0.016236904	Raspberr 58:e8:19	GOOSE
0.022705422	Raspberr 58:e8:19	GOOSE
0.023929671	Raspberr 58:e8:19	GOOSE
0.025194346	Raspberr 58:e8:19	GOOSE
0.039961654	Raspberr 73:92:52	GOOSE
0.041088202	Raspberr 73:92:52	GOOSE
0.042236935	Raspberr 73:92:52	GOOSE
0.125238563	Raspberr 58:e8:19	GOOSE
0.142271134	Raspberr 73:92:52	GOOSE



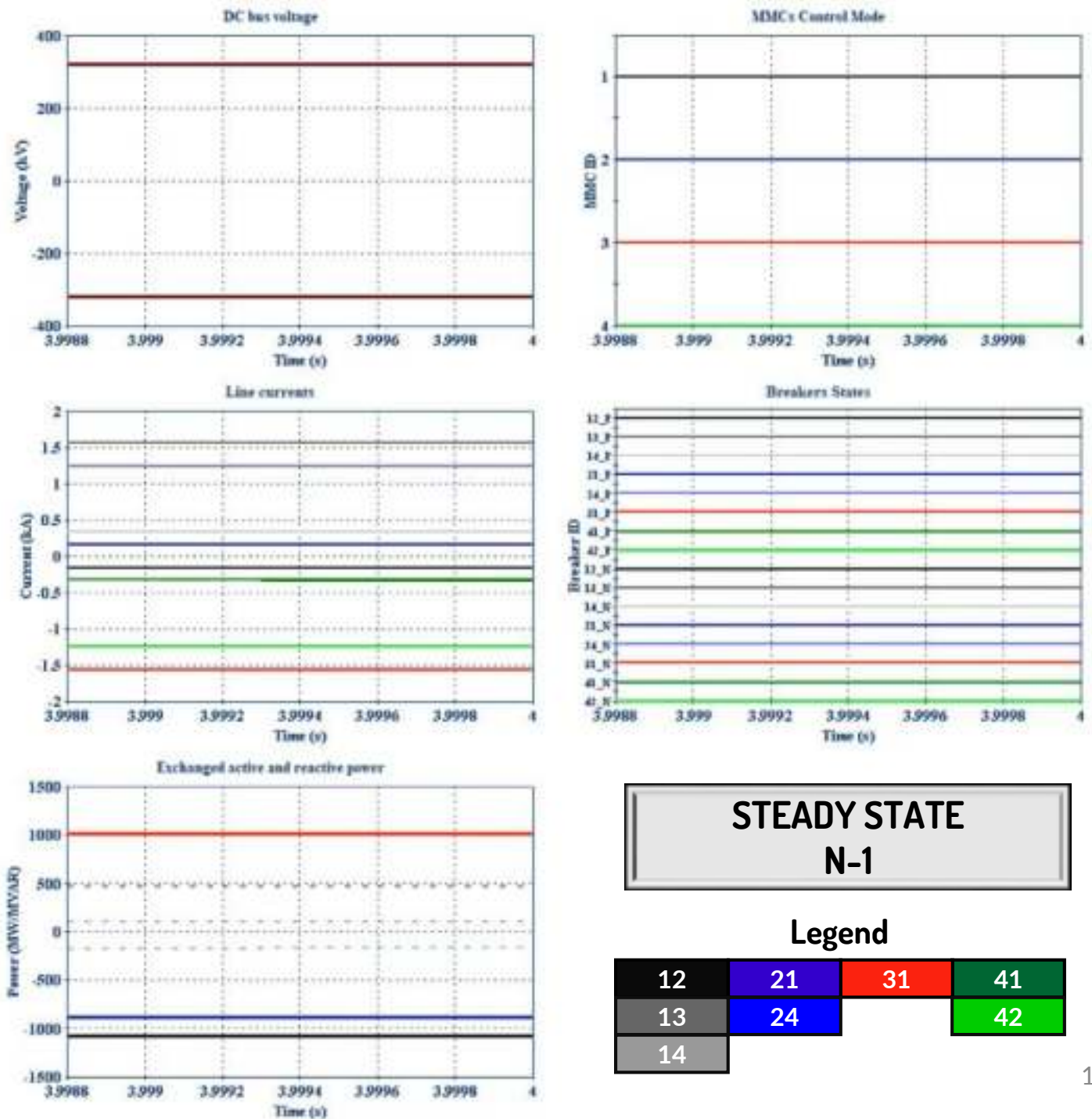
RESULTS OF THE HIL DEMONSTRATION

FULL-BRIDGE CONVERTER-BASED PROTECTION STRATEGY

Pole-to-pole fault: cable 24 (@50km)



¹ AC breaker module
² Modular multi-level converter
³ Line breaker module





Laurent Chédot

CONCLUSION

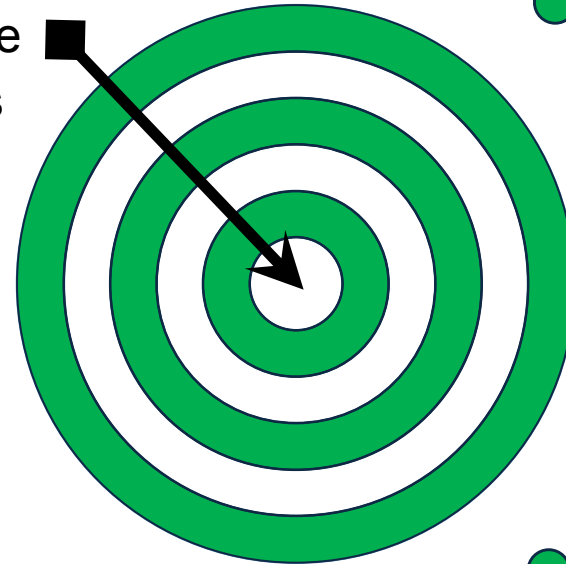


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RESULTS

HVDC protection Demonstration

Non-selective
schemes



HIL

Protection and Supervision IEDs tested

RTS model

HVDC breaker and MMC
models integrated to Hypersim

Benchmark grid

Two 4-terminal HVDC
networks implemented

Sequences validation

Primary and backup
sequences validated through HIL

Interoperability

Implementation of the IEC61850
industrial communication standard

Supervision

System supervision designed,
implemented and tested

CONCLUSION

NEXT STEPS

- KPI calculation
- Extensive testing
- IEDs maintenance
 - Protection
 - Supervision
- Benchmark grid evolution
- Robustness studies
 - Communication network
 - Restoration backup sequence → DC grid control upgrade

**Thank you for your attention. For further questions,
don't hesitate to contact me.**

**Check the demonstration at:
www.promotion-offshore.net**

North Sea Grid for the European New Deal

How to unlock Europe's Offshore Wind potential – a deployment plan for meshed HVDC grid

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