

Design & performance validation of 320kV HVDC spacer in GIS/GIL

1. Context

Due to the development of High Voltage Direct Current (HVDC) technology which is particularly suitable for the transmission of large amount of energy over long distances and for off-shore energy integration, new technology for HVDC Gas Insulated Switchgears (GIS) and Gas Insulated Lines (GIL) is developing thanks to its compactness and its high reliability for application in HVDC switchyard.

Development and dimensioning of HVDC GIL and GIS requires deep knowledge on electric field distribution in the gas/solid insulating systems. The electrical field distribution changes progressively from a capacitive state which depends only on permittivity to a resistive state which depends on permittivities and conductivities of gaseous and solid insulations. Moreover, various factors like the temperature gradient due to the nominal current, the charge carrier generation in gas due to the gas moistures or the roughness/imperfections of high voltage electrodes, the interface charge accumulation at the interfaces between gas/solid, the space charge accumulation inside solid spacer can influence strongly the electric field distribution and thus the withstand voltage and the reliability of the HVDC system.

For a reliable design of HVDC GIL/GIS, the phenomena understanding, the material's characteristics, the simulation methodology/model must be mastered in order to take into account the specific nonlinear properties of insulating materials and the specific phenomena at the operating conditions: high DC voltage and with temperature gradient.

2. Product proposal

SuperGrid Institute proposes a new design of spacer adapted for 320kV HVDC GIL/GIS. The new spacer and the busbar system was designed not only to satisfy all standard requirements such as mechanical, temperature rise, heating cycle performance but also particular requirements for HVDC applications such as superimposed impulse tests.

Type and aging tests according to CIGRE JWG D1/B3.57 were successfully conducted in an independent laboratory (EDF Les Renardières) to verify the insulating performance and the design of the 320kV HVDC GIL/GIS system. The satisfactory results confirm the high technology readiness level of HVDC GIL/GIS.

2.1. Specifications

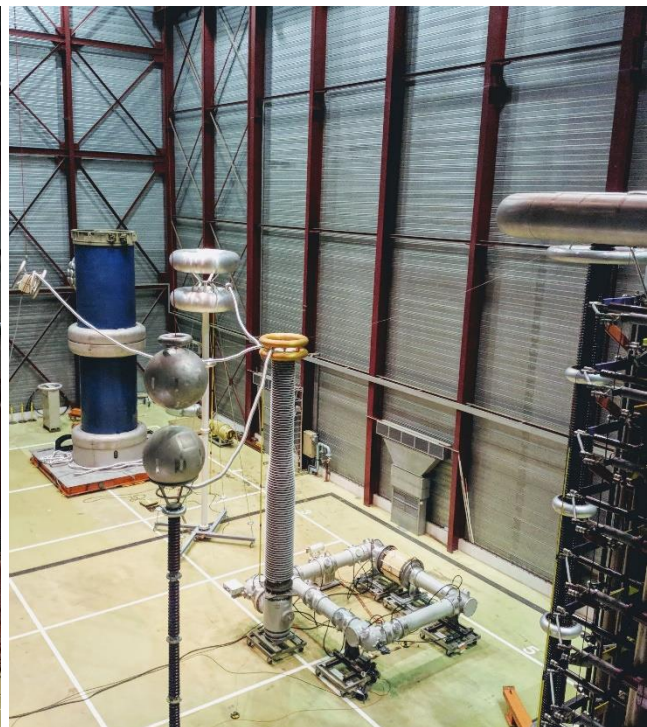
Rated voltage	320 kV
Rated continuous voltage	350 kV
Rated withstand voltage	528 kV
Rated current	4 kA
Rated lightning impulse	1050 kV
Rated switching impulse	950 kV

2.2. Main components

320 kV DC spacer and electrodes

T-housing

Disconnecter switch



Design & performance validation of 320kV HVDC spacer in GIS/GIL	GIRODET Alain	Page :2/5
	Autres mentions	

3. Deliverables

- Drawing files: 320kV DC spacer and busbar system
- Calculation note: 1303-vAA-Calculation note for 320kV DC spacer
 - SIMULATION SOFTWARE
 - SOURCE DATA
 - CRITERIA OF VALIDITY
 - DOMAIN OF VALIDITY
 - 1. PLAN
 - 2. SOURCE DATA
 - 3. ELECTRIC STRESS
 - 3.1. Ambient temperature
 - 3.1.1. Time constant
 - 3.1.2. Nominal DC voltage 320kV
 - 3.1.3. Rated withstand DC voltage 528kV
 - 3.1.4. Lightning superimposed impulse withstand voltage
 - 3.1.5. Switching superimposed impulse withstand voltage
 - 3.2. Temperature gradient
 - 3.2.1. Nominal DC voltage 320kV
 - 3.2.2. Rated DC withstand voltage 528kV
 - 3.2.3. Lightning superimposed impulse withstand voltage
 - 3.2.4. Switching superimposed impulse withstand voltage
 - 3.2.5. Switching superimposed impulse withstand voltage
 - 4. CONCLUSION
- Test report : 1029-vAA-320kV DC loop Temperature rise test
 - 1. INTRODUCTION
 - 2. TEST
 - 2.1. Test objects
 - 2.2. Test values
 - 2.3. Instrumentation
 - 3. TEST PREPARATION – CONTACT RESISTANCES
 - 4. TEST RESULTS
 - 4.1. Temperature rise
 - 4.2. Time constant
 - 4.3. Overload calculation
 - 4.4. Mapping of temperature rise
 - 4.4.1. 3150A
 - 4.4.2. 4000A
 - 4.4.3. 4300A

Design & performance validation of 320kV HVDC spacer in GIS/GIL	GIRODET Alain	Page :3/5
	Autres mentions	

- 4.4.4. 4600A
 - 4.5. Analyze
 - 5. CONCLUSIONS
 - 6. ANNEXES

- Test report: 1276-vAA-320kV DC spacer Preliminary test
 - 1. INTRODUCTION
 - 2. SPECIFICATION DU SYSTEME
 - 3. OBJET EN ESSAI
 - 4. EXPERIMENTATIONS
 - 4.1. Essai thermique
 - 4.1.1. Essai
 - 4.1.2. Grandeurs d'essais
 - 4.1.3. Instrumentation de l'appareil
 - 4.1.4. Procédure d'essai
 - 4.1.5. Préparation des essais : mesure de résistance de contact
 - 4.1.6. Synthèse des résultats
 - 4.1.7. Déterminant de l'exposant appareil & estimation de l'échauffement à 4000A sous SF6
 - 4.1.8. Conclusion
 - 4.2. Essai mécanique
 - 4.2.1. Essai de rupture en pression
 - 4.2.2. Essai en flexion
 - 4.3. Essai diélectrique
 - 4.3.1. But d'essai
 - 4.3.2. Objet en essai
 - 4.3.3. Séries d'essais
 - 4.3.4. Préparation des essais
 - 4.3.5. Résultats des essais
 - 4.3.6. Comparaison entre résultats d'essai et simulation
 - 4.3.7. Conclusion
 - 5. CONCLUSION

- Test report: 1607-vAA-Performance of 320kV DC spacers Load cycle tests
 - 1. INTRODUCTION
 - 2. TEST
 - 2.1. Test object
 - 2.2. Test procedure
 - 2.3. Validity criteria
 - 3. RESULTS

Design & performance validation of 320kV HVDC spacer in GIS/GIL	GIRODET Alain	Page :4/5
	Autres mentions	

- 3.1. PD measurement before thermal cycle
 - 3.2. PD measurement after thermal cycle
 - 4. CONCLUSION
- Test report: 320kV DC loop Type test report (EDF Renardières report **HM-22/08-2015-0226/1**)
 - 1. REFERENCE DOCUMENTS
 - 2. APPARATUS FEATURES DECLARED BY THE MANUFACTURER
 - 3. LIST OF TESTS PERFORMED
 - 4. INTRODUCTION
 - 5. TEST CONDITIONS
 - 6. IDENTIFICATION OF TESTED OBJECT
 - 7. MEASUREMENT UNCERTAINTIES
 - 8. TESTS RESULTS
 - 8.1. Preliminary PD Tests
 - 8.2. AC withstand dielectric test
 - 8.3. DC withstand dielectric tests
 - 8.4. Superimposed LI impulse with DC voltage
 - 8.5. Superimposed SI impulse with DC voltage
 - 8.6. PD Tests after superimposed tests
 - 8.7. DC withstand dielectric tests
 - 8.8. Combined voltage test
 - 8.9. Load condition tests – Superimposed LI impulse DC positive voltage
 - 8.10. Load condition tests – Superimposed SI impulse with DC positive voltage
 - 8.11. Load condition tests – Superimposed SI impulse with DC negative voltage
 - 8.12. Load condition tests – Superimposed LI impulse with DC negative voltage
- Test report: 320kV DC loop Aging test report (EDF Renardières report)
 - 1. REFERENCE DOCUMENTS
 - 2. APPARATUS FEATURES DECLARED BY THE MANUFACTURER
 - 3. LIST OF TESTS PERFORMED
 - 4. INTRODUCTION
 - 5. TEST CONDITIONS
 - 6. IDENTIFICATION OF TESTED OBJECT
 - 7. MEASUREMENT UNCERTAINTIES
 - 8. TESTS RESULTS

Design & performance validation of 320kV HVDC spacer in GIS/GIL	GIRODET Alain	Page :5/5
	Autres mentions	