Low level FPGA MMC control

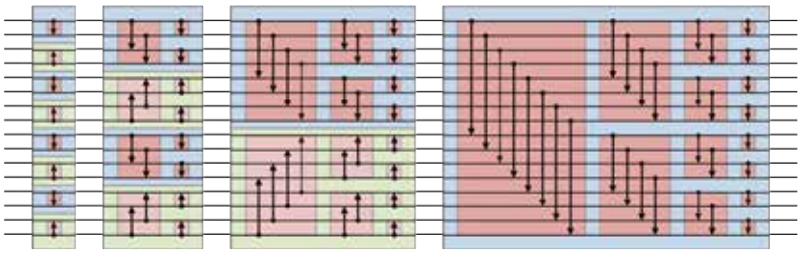
Pipelined bitonic sorting implemented on FPGA

CONTEXT

Low level control of Multilevel Modular Converters (MMC) consists in realizing the arms voltage set point while maintaining a balanced state of charge of the submodules capacitors. This process is repetitive, its time step being in the order of magnitude of decades of microseconds. Depending on the arm current direction, the inserted submodules may charge or discharge. For example, in case of a charging current, the submodules with the lower voltages should be inserted in priority. Many techniques exist, reaching different levels of compromise between mean switching frequency and the amplitude of the voltage ripple for each submodules.

TECHNOLOGY DESCRIPTION

The best information to make the right selection at each time step is a sorted list of the submodules according their capacitor voltage value. Easier said than done, it is a challenge to sort 512 values in microseconds for all 6 arms.



Implemented on Xilinx FPGA, a low level control using a full sort is proposed. The Bitonic sorting algorithm is suited to FPGA due to is parallel nature. But in this case where 6 times 512 values have to be sorted, a direct implementation requires more space than available on the FPGA. We overcame this problem by pipelining the process, using the modular nature of the algorithm.

APPLICATION DOMAIN

MMC converter control

ADVANTAGES

Full sorting

6 times 512 levels

Tested in HIL

TRL SCALE

1 2 3 4 5 6 7 8 9

DELIVERABLES

Firmware source - Full sorting for 256 modules (512 targeted) on VIRTEX7 FPGA
Technical support